ECSE 487

# A RTL-Level Implementation of a Pipelined RISC CPU Core

Report submitted to Professor Warren Gross

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## DESCRIPTION

This assignment consisted of a VHDL implementation of a simplified version of the MIPS-64 architecture. MIPS-64 is one of the later versions of the well established family of RISC type architecture known as MIPS. As its name indicates, MIPS-64 is a 64 bit version of the base MIPS architecture. The minimum requirements for this assignment were to design and implement a 5-stage pipelined version of the MIPS-64 processor that would support a reduced set of instructions consisting of:

*NOP, LD, SD, DADD, DADDI, DADDU, DADDUI, DSUB, DSUBI, DSUBU, DSUBUI, AND, ANDI OR, ORI, XOR, XORI, DSLL, DSRL*

The datapath and control unit were required to handle only the execution of the given instructions, while other parts of the processor were not of concern. Adding to the sophistication of the design was the requirement to handle hazards associated with pipelined architectures.

While there are a great number of ways of implementing MIPS-64 architectures, a key aspect of this assignment was to choose a design with pipelining efficiency in mind. This means that pipelining should be integrated into the design right from the start, as opposed to being added as an afterthought. The other area of the assignment requiring careful planning was the design of the hazard detection and handling protocols.

## METHODOLOGY

### Datapath

#### Single-Cycle vs. Multi-Cycle

The datapath design was a classic 5 stage multi-cycle MIPS-64 architecture. Instead of initially implementing a non-pipelined datapath which would then be modified for pipelining, the datapath was designed right from the start to support pipelining. MIPS-64 architectures can be implemented in with either single-cycle or multi-cycle datapaths. The multi-cycle implementation is a better choice because it is superior in both performance and hardware costs. A single-cycle implementation's CPI of 1 is misleading since the clock cycle is determined by the instruction with the largest latency. Thus many instructions that could be completed with shorter clock cycles must still take up unnecessary time. This dependence on the slowest instruction violates the fundamental design principle of making the common case fast. The high hardware cost comes from the fact that since each functional unit can only be used once per clock cycle, certain functional units must be duplicated. The multi-cycle implementation is similar to simpler MIPS-64 implementations in that is still retains most of the same major functional units (PC, ALU, etc), but key differences are that many of these components are now shared and the addition of registers to hold the output of one stage until it is required by a future stage.

## Overall View

The datapath was split into the following five stages: the Instructions Fetch (**IF**) stage, the Instruction Decode (**ID**) and register file read stage, the Execution (**EX**) or address calculation stage, the data Memory (**MEM**) access stage and the Write Back (**WB**) stage. Having the datapath split into these five stages means that up to five instructions are executing during any single clock cycle. Non-pipelined multi-cycle designs require several temporary registers to store outputs of functional units for future use, but pipelined datapaths integrate the functions of those temporary registers into generalized pipeline registers placed in between pipe stages. An image of the basic datapath is displayed in figure 1.

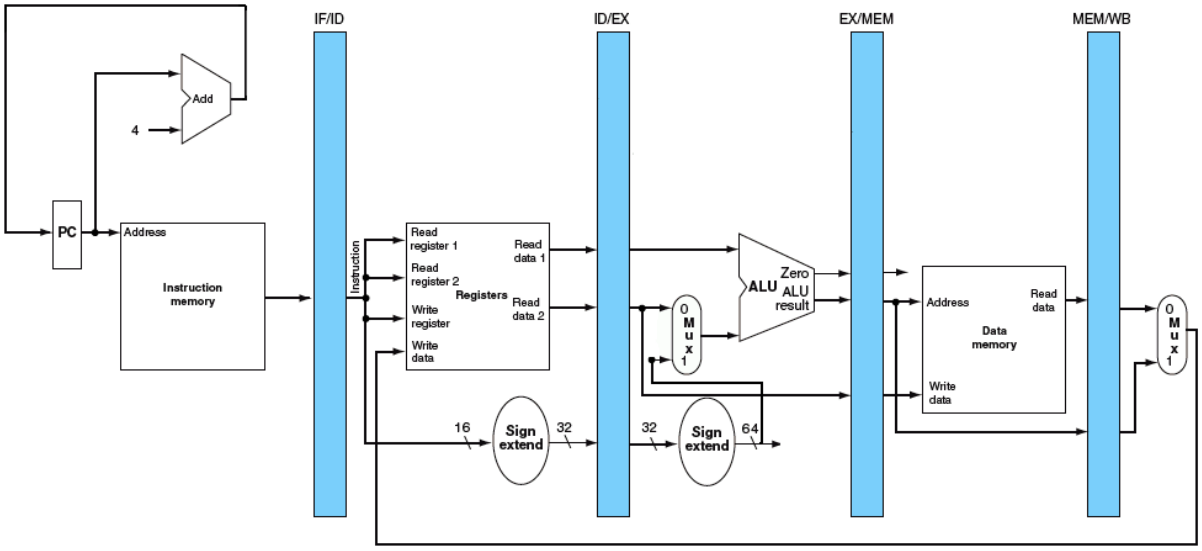


**Figure 1 Basic Datapath:** **This image does not contain every component of the final datapath, it serves to highlight the essential components of the datapath not pertaining to control or hazards. [1]**

## IF

Under normal operating conditions, the PC is incremented by 4 at every clock pulses and the next instructions presented at the output port of the IF stage. If a hazard is detected, the PC stops incrementing until the hazard condition has passed. (The instruction at the output doesn't matter since the IF/ID register is in memory mode, trapping the "hazardous" instruction until it is safe to execute).

## ID

The ID stage takes the output instruction from the IF/ID register. The instruction is both read by the controller (for decoding and conversion into appropriate control signals for the pipeline components) and by the register unit. Regardless of whether it is needed or not, the ports 'Read register 1' and 'Read register 2' are loaded with the data inside the registers addressed by 'instruction bits 25 to 21' and 'instruction bits 20 to 16' respectively. The control signal RegDst

selects which register will be written at the WB stage and presents the data to the ID/EX register. This stage also sign extends the 16 bit immediate field onto a 32-bits signal.

**EX**

The EX stage adds the data from Read data 1 with either the data from Read data 2 or with a sign extended immediate. The sign-extended immediate comes from the ID/EX pipeline register, but is sign extended a second time to produce a 64 bit input. If reset is not asserted, this stage selects the proper ALU operation depending of the ALUOp parameter and the Opcode (instruction bits 31 to 26). Instructions are split into two major categories, I-type and R-Type. The ALU is utilized to perform arithmetic operations or to calculate memory addresses.

**MEM**

The MEM stage is where any memory addresses computed in the EX stage are used to read data from memory or to write data to memory. Read data is then loaded into the MEM/WB pipeline register. Again, C code was utilized to produce memory locations and all applicable cases.

**WB**

In the WB stage, any data that had been read in the MEM stage or computed in the EX stage is sent back to the registers where it is written if RegWrite is asserted. The target register is read from the 'WriteReg' port (Target was originally selected in this unit, but outputted to the pipeline for aging to arrive within good stage timing since the WB stage is not clicked)

**Main Control Unit**

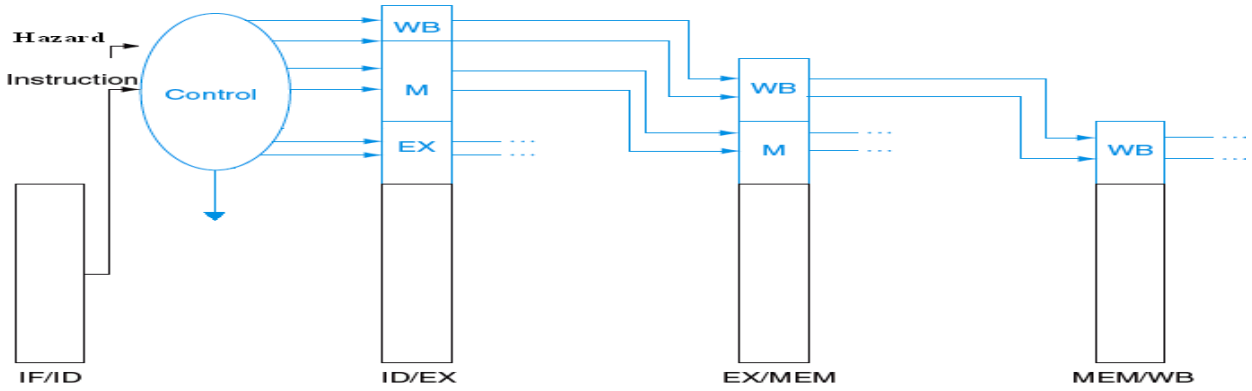


Figure 2 High Level Control Unit Propagation [1]

The Main Control Unit (MCU) is responsible for coordinating all data flow in the datapath. Its main input is the instructions itself, although in theory the MCU is concerned mainly with the Opcode (bits 31 to 26). The control lines being utilized in this design are: RegDst, ALUOp, ALUSrcB, MemRead, MemWrite, RegWrite, and MemtoReg.

The control lines are immediately asynchronously set according to the instruction presented to the MCU by the IF/ID register. Due to pipelining, the control signals for a given instruction are fed to the ID stage, and then propagated through registers such that a they follow

the data they control through the pipeline and subsequent stages will only receive their appropriate control signal when they are processing the pertinent instruction. This process is displayed in figure 2.

The MCU also has a hazard detected input coming from the HDU which is directly fed back to a hazard detected port. This signal is forwarded to all relevant pipe stages. The hazard detection unit could have sent the hazard assert signal to the other functional units directly, but the reasoning behind this design decision was to keep all control related activities centralized in the MCU. The full control datapath complete with hazard control lines is displayed in figure 3.

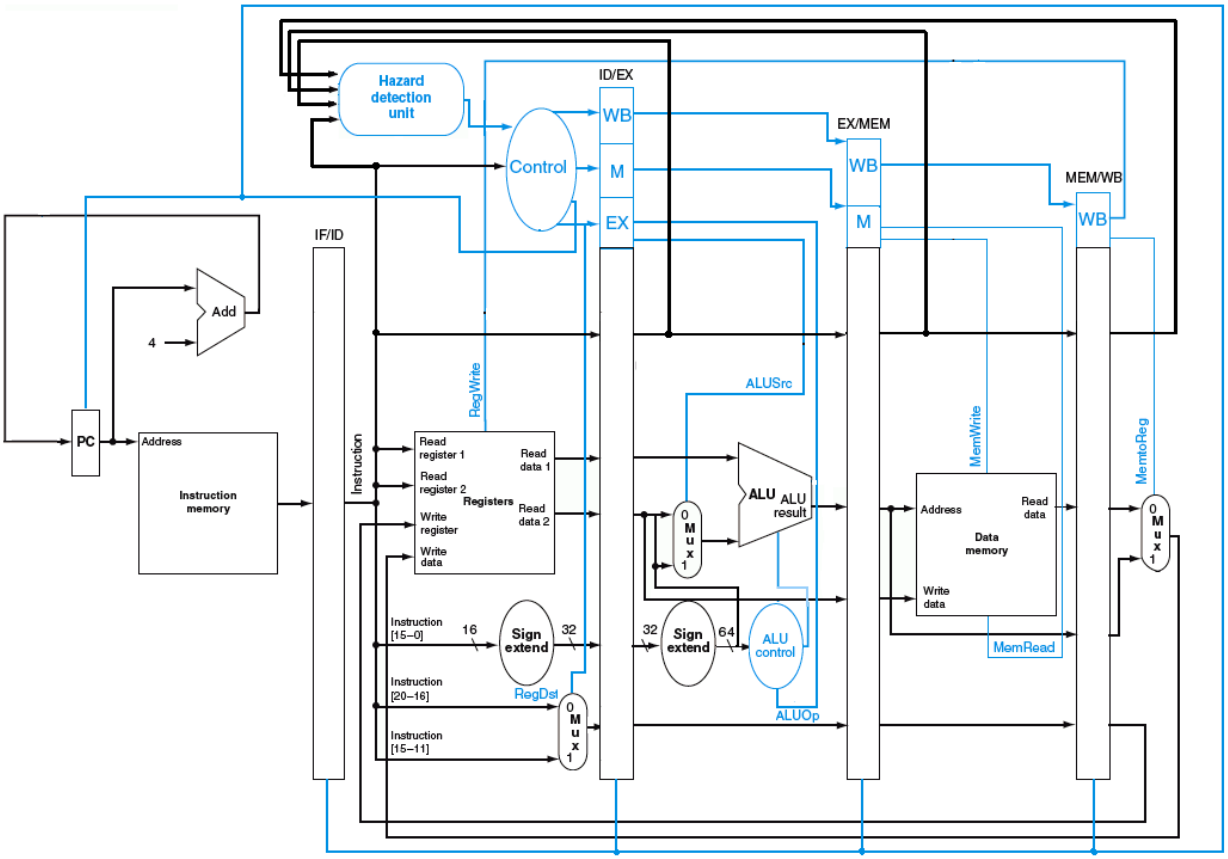


Figure 3 Full Control Datapath [1]

## Pipelining

As previously mentioned, this implementation of MIPS-64 was designed to be pipelined and as such pipeline hardware was an intricate part of the datapath. The key concepts here were the efficient splitting of the datapath into stages and the design of the pipeline registers which manage the flow of data between pipe stages. While the pipeline stages themselves are independent of the clock, the pipe registers ensure that data from a previous stage is provided to the following pipe stage upon the next clock cycle. Every register reads the previous stage's instruction and passes it on to the next register. This is done such that the HDU can simply read the instruction being executed at every pipeline stages and detect hazards. Each Register is also fed with a hazard control signal to force appropriate hazard recovery mechanisms if need be. The following section will provide some details on each specific pipe register. Please refer to figure 3 for clarification.

### IF/ID Register

The IF/ID register is responsible for providing the instruction fetched in the IF stage as an input to the ID stage.

### ID/EX Register

The ID/EX register is the one that starts the propagation of the control signals. It splits the control signals into three categories: EX, MEM and WB. Signals from the EX group (RegDst, ALUOp and ALUSrcB) will be consumed in the very next stage, while MEM and WB signal are simply passed to the next pipe register (EX/MEM register). It also propagates the two data units read from the registers, the extended input and the future value of the write register.

### EX/MEM Register

The EX/MEM register propagates the WB control signals to the next pipe register, while delivering the MEM control signals (MemRead and MemWrite) to their respective functional units. In addition, the ALU result, the read value of register B and the future value of the write register are propagated.

### MEM/WB Register

The MEM/WB register delivers the WB control signals (RegWrite, and MemtoReg) to their respective functional units, as well as providing the ALU result, the read memory data and the future value of the write register.

## Hazard Detection

The hazard detection unit reads the instructions being operated at every stage from the data registers. It contains a hard wired list of all possible hazard conditions and as soon as a hazard instruction is detected in the ID stage, the HDU responds. The first thing it does is to stop the PC from incrementing and sets the ID/IF register into memory mode. The instruction present in the ID/IF register (which caused the hazard) will still be decoded, but the resulting data and control lines will never be read since the IF/EX register stops reading its input and fires NOP until the

hazard has passed. This enables all the data downstream from the IF/EX register to continue being processed until the hazard has passed, while being followed by NOPs in order to avoid any data corruption. Once the hazard has passed, the HDU advises the controller to de-assert the hazard line. In the IF stage, PC will get incremented at the next clock pulse and the next instruction will be sent out. The instruction which caused the hazard that was to be executed next has already been decoded, so the ID/EX register simply has to stop firing NOPs and start reading it's inputs again to put the pipeline back to normal operation.

| Consumer | Producer | Status |
|---|---|---|
| ALU | ALU | OK |
| ALU | ALU Immediate | OK |
| ALU | Load | OK same as ALU - ALUImm |
| ALU | Store | No Hazads Possible |
| ALU Immediate | ALU | OK |
| ALU Immediate | ALU Immediate | OK |
| ALU Immediate | Load | OK same as ALUImm - ALUImm |
| ALU Immediate | Store | No Hazads Possible |
| Load | ALU | OK same as ALUImm - ALU |
| Load | ALU Immediate | OK same as ALUImm - ALUImm |
| Load | Load | OK same as ALUImm - ALUImm |
| Load | Store | No Hazads Possible |
| Store | ALU | OK same as ALUImm - ALU |
| Store | ALU Immediate | OK same as ALUImm - ALUImm |
| Store | Load | OK same as ALUImm - ALUImm |
| Store | Store | No Hazads Possible |

Table 1 Hazard Detection Look-Up Table

## TESTBENCH

A synthesizable test bench was written and implemented in the IF stage. Its purpose was to generate a sequence of instructions that would highlight corner cases. The following table presents the sequence of instructions that were used for the testbench simulation:

| | Instruction |
|---|---|
| 1 | DADDI : Reg1 <- Reg0 + (-1) |
| 2 | DADDIU : Reg2 <- Reg1 + 1 |
| 3 | DSUBI : Reg3 <- Reg2 - (-1) |
| 4 | DSUBIU : Reg4 <- Reg3 - 1 |
| 5 | ORI : Reg5 <- Reg4 OR "1010101010101010" |
| 6 | ANDI : Reg6 <- Reg5 AND "0000000011111111" |
| 7 | XOR : Reg7 <- Reg6 XOR "1111111111111111" |
| 8 | SD : memory(Reg2 + 0) <- Reg5 |

| | |
|---|---|
| 9 | LD : Reg8 <- memory(Reg2 + 0) |
| 10 | DADD : Reg9 <- Reg3 + Reg1 |
| 11 | DADDU : Reg10 <- Reg3 + Reg5 |
| 12 | DSUB : Reg11 <- Reg0 - Reg1 |
| 13 | DSUBU : Reg12 <- Reg10 - Reg3 |
| 14 | AND : Reg13 <- Reg5 AND Reg1 |
| 15 | OR : Reg14 <- Reg12 OR Reg11 |
| 16 | XOR : Reg15 <- Reg14 XOR Reg5 |
| 17 | DSLL : Reg16 <- Reg15 << 1 |
| 18 | DSLL : Reg17 <- Reg16 >> 1 |

Table 2: Sequence of instruction used for simulation

## SIMULATION RESULTS

Figures 4 to 9 show the simulation results for the instructions in table 2. In figure 4, once the reset signal is de-asserted, instruction 1 (DADDI) is fetched at the rising edge of the next clock cycle. In the following clock cycle, instruction 2 (DADDIU) is fetched while instruction 1 is in the ID stage. Once instruction 2 enters the ID stage, it is fed to the hazard detection unit and the main controller unit. A potential hazard is then detected, which instructs the PC to stop incrementing, the IF/ID pipeline register to go into memory mode, and the ID/EX pipeline register to generate a NOP. This NOP will be cascaded from one pipeline register to another, like a bubble. This process continues until the instruction 1's destination register is written, at which point instruction 2 may proceed. An example of a non-hazardous combination of instructions can be seen in figure 6, where the tenth instruction (DADD) operates on source registers that have already been written by their respective instructions. As a consequence, it can be seen that the IF/ID pipeline register is not in memory mode and that the hazard control signal is de-asserted.

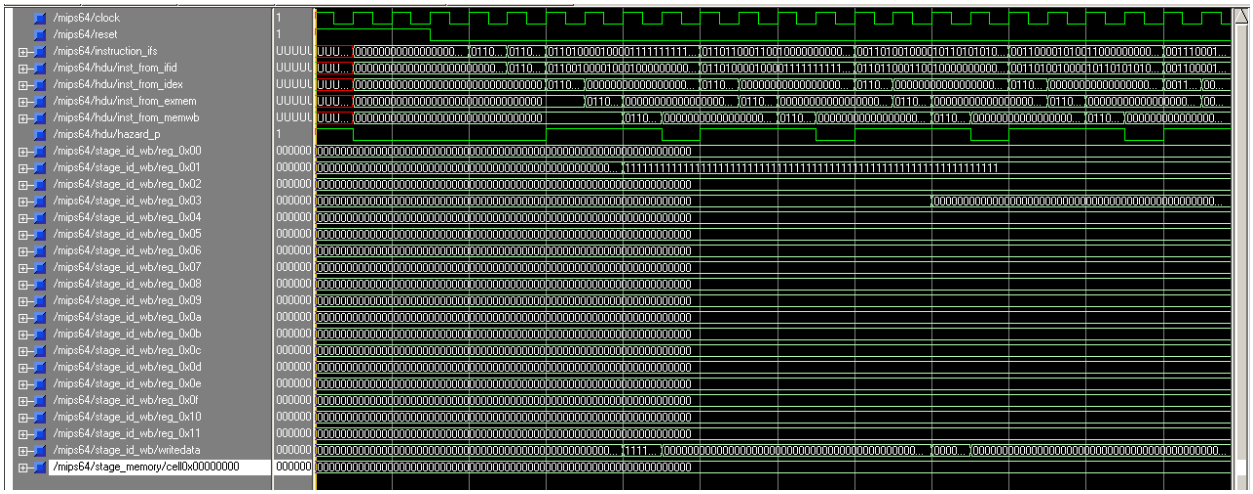


Figure 4 Simulation Screenshot 1

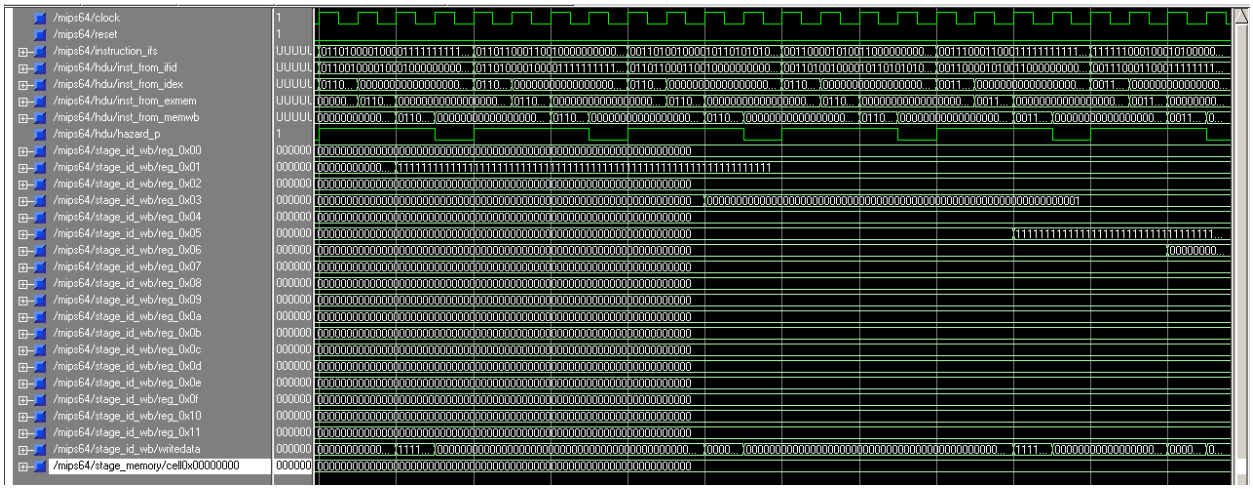


Figure 5 Simulation Screenshot 2

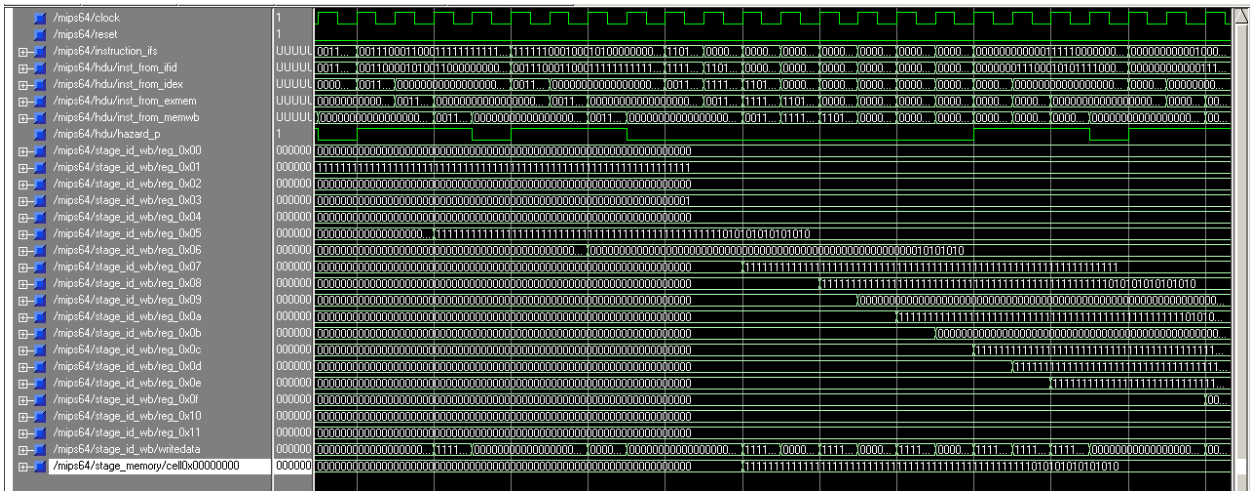


Figure 6 Simulation Screenshot 3

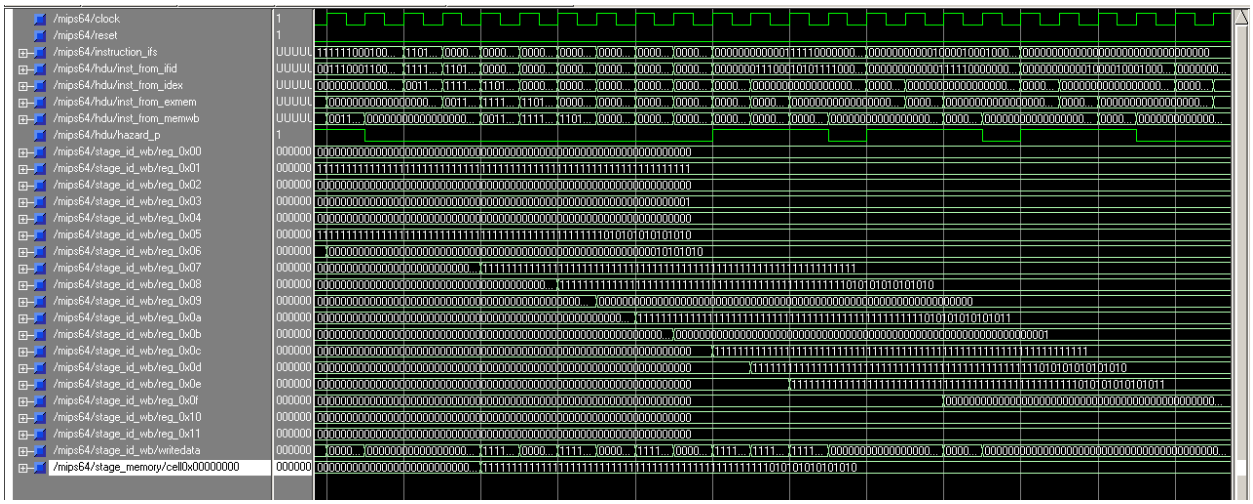


Figure 7 Simulation Screenshot 4

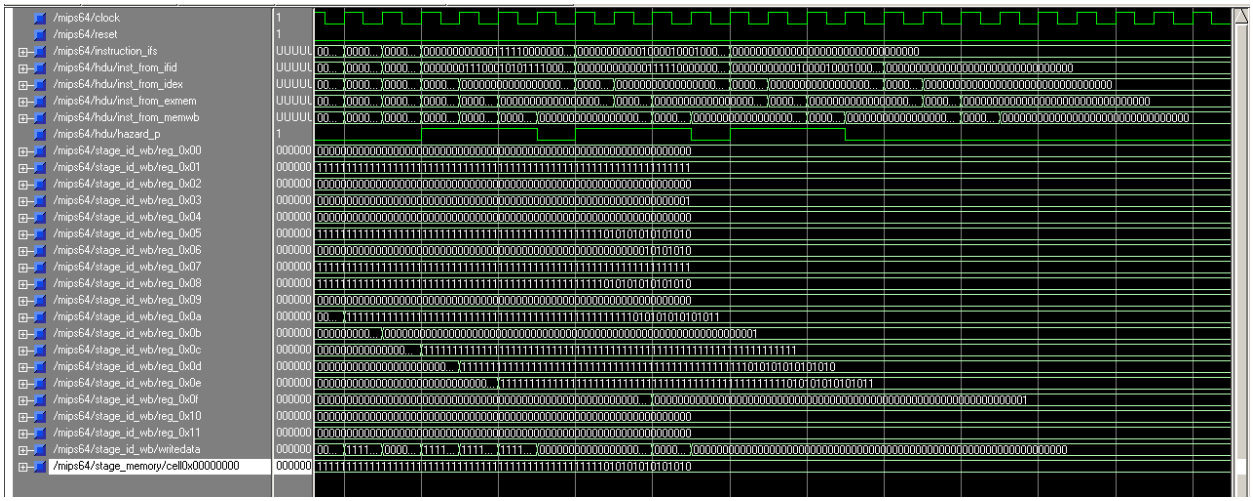


Figure 8 Simulation Screenshot 5

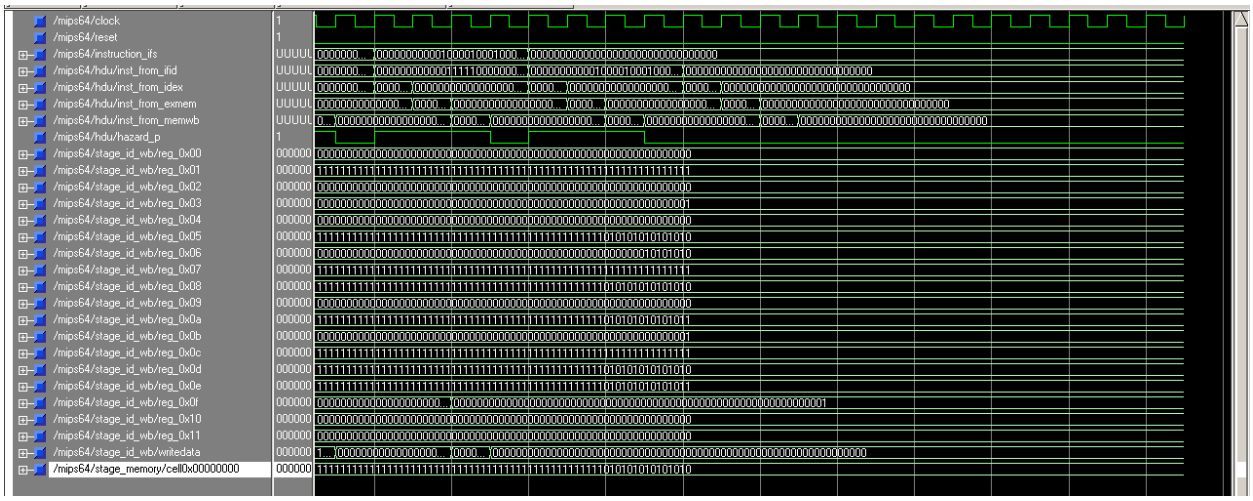


Figure 9 Simulation Screenshot 6

## SYNTHESIS

| Component/Stage Name | Clock Frequency (MHz) | Critical Path (ns) |
|---|---|---|
| HDU | 110 | 0.89 |
| Controller | 154 | 3.51 |
| IF Stage | 180 | 4.46 |
| ID/WB Stage | 174 | 4.26 |
| EX Stage | 110 | 0.97 |
| MEM Stage | 150 | 1.92 |

Table 3 Frequency and Critical Path Table

Since the clock can only be as fast as the slowest pipeline stage, the maximum frequency that can be utilized for this MIPS-64 design is 110 MHz. The critical path is equal the summation of each stages's critical path and the result is 16.01.

| Component / Stage Name | IOs (%) | Global Buffers (%) | Function Generators (%) | CLB Slices (%) | DFFs or Latches (%) | Block RAMs (%) | Block Multiplier (%) | Block Multiplier DFFs (%) |
|---|---|---|---|---|---|---|---|---|
| HDU | 221.59 | 0.00 | 18.23 | 18.23 | 0.00 | 0.00 | 0.00 | 0.00 |
| Controller | 46.59 | 0.00 | 1.76 | 1.95 | 0.00 | 0.00 | 0.00 | 0.00 |
| IF Stage | 38.64 | 6.25 | 2.54 | 7.03 | 4.64 | 0.00 | 0.00 | 0.00 |
| ID/WB Stage | 372.73 | 0.00 | 446.09 | 446.09 | 255.67 | 0.00 | 0.00 | 0.00 |
| EX Stage | 294.32 | 0.00 | 298.05 | 298.05 | 0.00 | 0.00 | 0.00 | 0.00 |
| MEM Stage | 220.45 | 6.25 | 16.80 | 25.00 | 16.49 | 0.00 | 0.00 | 0.00 |

Table 4 Hardware Utilization Table

For the complete synthesis reports please see Appendix.

## DISCUSSION

The requirements for this assignment, implementing a five stage MIPS-64 pipeline, were successfully implemented for the most part. The final implementation of the design produced a multi-cycle, 5 stage pipeline, complete with a main controlling unit and a hazard detection unit. However the main weakness of this implementation is the handling of hazards. While the hazard detection unit has an efficient and elegant way of detecting the hazards, it is the handling of these hazards which is on the primitive side. The method of stalling until it is safe to proceed while simple, yields poor performance results. One obvious solution would have been to implement a forwarding mechanism, but time constraints did not allow for this feature to be added to the final implementation.

## REFERENCE

[1] Figures based on "Computer Organization and Design" 3rd Edition, David Patterson and John Hennessy, Morgan Kaufmann, 2005.

## APPENDIX

## HDU

### Hardware

```
************************************************
Device Utilization for 2V40cs144
************************************************
Resource             Used    Avail   Utilization
-------------------------------------------------
IOs                  129     88      146.59%
Global Buffers       0       16      0.00%
Function Generators  80      512     15.63%
CLB Slices           40      256     15.63%
Dffs or Latches      0       776     0.00%
Block RAMs           0       4       0.00%
Block Multipliers    0       4       0.00%
Block Multiplier Dffs  0     144     0.00%

-------------------------------------------------
WARNING: This design does not fit in the device specified!
Recommending to try an alternate device ...
************************************************
Device Utilization for 2V250fg256
************************************************
Resource             Used    Avail   Utilization
-------------------------------------------------
IOs                  129     172     75.00%
Global Buffers       0       16      0.00%
Function Generators  80      3072    2.60%
CLB Slices           40      1536    2.60%
Dffs or Latches      0       3588    0.00%
Block RAMs           0       24      0.00%
Block Multipliers    0       24      0.00%
Block Multiplier Dffs  0     864     0.00%

-------------------------------------------------

************************************************************

Library: work    Cell: hazard_detection    View: implementation
```

**********

| Cell | Library | References | Total Area |
|---|---|---|---|
| GND | xcv2 | 1 x | |
| IBUF | xcv2 | 64 x | |
| LUT2 | xcv2 | 3 x 1 | 3 Function Generators |
| LUT2_L | xcv2 | 12 x 1 | 12 Function Generators |
| LUT3 | xcv2 | 7 x 1 | 7 Function Generators |
| LUT4 | xcv2 | 34 x 1 | 34 Function Generators |
| LUT4_L | xcv2 | 24 x 1 | 24 Function Generators |
| MUXCY | xcv2 | 12 x 1 | 12 MUX CARRYs |
| MUXCY_L | xcv2 | 24 x 1 | 24 MUX CARRYs |
| MUXF5 | xcv2 | 9 x 1 | 9 MUXF5 |
| OBUF | xcv2 | 1 x | |
| VCC | xcv2 | 1 x | |

Number of ports : 129
Number of nets : 256
Number of instances : 192
Number of references to this view : 0

Total accumulated area :
Number of Function Generators : 80
Number of MUX CARRYs : 36
Number of MUXF5 : 9
Number of gates : 80
Number of accumulated instances : 192

**Timing**

CTE Report
Summary

Clock Frequency Report

| Domain | Clock Name | Min Period (Freq) |
|---|---|---|
| Design_Clock | Design_Clock | 9.111 (109.757 MHz) |

End CTE Report Summary ..... CPU Time Used: 0 sec.
#NAME?
CTE Report
Summary

Analyzing setup constraint violations 10

Setup Slack Path Summary

| Index | Setup Slack | Path Delay | Source Clock | Dest. Clock | Data Start Pin | Data End Pin | Edge |
|---|---|---|---|---|---|---|---|
| 1 | 0.889 | 9.111 | Design_Clock | Design_Clock | INST_FROM_MEMWB(20) | hazard_p | Rise |
| 2 | 0.889 | 9.111 | Design_Clock | Design_Clock | INST_FROM_MEMWB(19) | hazard_p | Rise |
| 3 | 0.972 | 9.028 | Design_Clock | Design_Clock | INST_FROM_MEMWB(18) | hazard_p | Rise |
| 4 | 0.972 | 9.028 | Design_Clock | Design_Clock | INST_FROM_MEMWB(17) | hazard_p | Rise |
| 5 | 1.028 | 8.972 | Design_Clock | Design_Clock | INST_FROM_IFID(25) | hazard_p | Rise |
| 6 | 1.028 | 8.972 | Design_Clock | Design_Clock | INST_FROM_IFID(24) | hazard_p | Rise |
| 7 | 1.111 | 8.889 | Design_Clock | Design_Clock | INST_FROM_IFID(23) | hazard_p | Rise |
| 8 | 1.111 | 8.889 | Design_Clock | Design_Clock | INST_FROM_IFID(22) | hazard_p | Rise |
| 9 | 1.357 | 8.643 | Design_Clock | Design_Clock | INST_FROM_EXMEM(18) | hazard_p | Rise |
| 10 | 1.357 | 8.643 | Design_Clock | Design_Clock | INST_FROM_EXMEM(17) | hazard_p | Rise |

End CTE Report Summary ..... CPU Time Used: 0 sec.
#NAME?
CTE Critical Path Report
-- CTE get true worst setup path..

Critical path #1, (path slack = 0.89):

SOURCE CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 1st rising edge
DEST CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 2nd rising edge

| NAME | GATE | DELAY | ARRIVAL | DIR | FANOUT |
|---|---|---|---|---|---|
| INST_FROM_MEMWB(20) | (port) | | 0.00 | dn | |
| INST_FROM_MEMWB(20) | (net) | 0.00 | | | 1 |
| INST_FROM_MEMWB_ibuf(20)/I | IBUF(LVTTL) | | 0.00 | dn | |
| INST_FROM_MEMWB_ibuf(20)/O | IBUF(LVTTL) | 0.95 | 0.95 | dn | |
| INST_FROM_MEMWB_int(20) | (net) | 0.00 | | | 3 |

i10bcx96/I1 LUT4_L 0.95 dn
i10bcx96/LO LUT4_L 0.35 1.30 up
n10bcx92 (net) 0.00 1
i10bcx95/S MUXCY_L 1.30 up
i10bcx95/LO MUXCY_L 0.36 1.66 up
n10bcx91 (net) 0.00 1
i10bcx94/CI MUXCY_L 1.66 up
i10bcx94/LO MUXCY_L 0.04 1.70 up
n10bcx90 (net) 0.00 1
i10bcx93/CI MUXCY 1.70 up
i10bcx93/O MUXCY 0.86 2.56 up
a(0) (net) 0.00 2
i10bcx105/I0 LUT4 2.56 up
i10bcx105/O LUT4 0.49 3.04 dn
n10bcx100 (net) 0.00 1
i10bcx101/I3 LUT4 3.04 dn
i10bcx101/O LUT4 0.49 3.53 up
n10bcx97 (net) 0.00 1
i10bcx100/S MUXF5 3.53 up
i10bcx100/O MUXF5 0.69 4.22 up
n10bcx96 (net) 0.00 1
i10bcx99/S MUXF5 4.22 up
i10bcx99/O MUXF5 0.69 4.91 up
n10bcx95 (net) 0.00 1
i10bcx86/I3 LUT4 4.91 up
i10bcx86/O LUT4 0.49 5.40 up
n10bcx83 (net) 0.00 1
i10bcx65/I1 MUXF5 5.40 up
i10bcx65/O MUXF5 0.51 5.91 up
n10bcx62 (net) 0.00 1
i10bcx52/I3 LUT4 5.91 up
i10bcx52/O LUT4 0.49 6.40 up
n10bcx49 (net) 0.00 1
i10bcx34/I1 MUXF5 6.40 up
i10bcx34/O MUXF5 0.51 6.91 up
n10bcx32 (net) 0.00 1
i10bcx21/I3 LUT4 6.91 up
i10bcx21/O LUT4 0.49 7.40 up
n10bcx19 (net) 0.00 1
i10bcx1/I1 MUXF5 7.40 up
i10bcx1/O MUXF5 0.51 7.91 up
hazard_p_dup0 (net) 0.00 1
hazard_p_obuf/I OBUF(LVTTL,FAST,24) 7.91 up

```
hazard_p_obuf/O        OBUF(LVTTL,FAST,24)      1.20     9.11   up
hazard_p               (net)                    0.00        0
hazard_p               (port)                             9.11   up

                                    Initial edge separation:     10.00
                                    Source clock delay:     -
                                    0.00
                                    Dest clock delay:       +
                                    0.00
                                                 ----------
                                    Edge separation:
                                    10.00
                                    Setup constraint:       -
                                    0.00
                                                 ----------
                                    Data required time:          10.00
                                    Data arrival time:      -
                                    9.11
                                                 ----------
                                    Slack:                   0.89

-- CPU Time Used: 0 sec.
End CTE Analysis ..... CPU Time Used: 0 sec.
```

## Controller

### Hardware

```
**********************************************
Device Utilization for 2V40cs144
**********************************************
Resource             Used    Avail   Utilization
-----------------------------------------------
IOs                  41      88      46.59%
Global Buffers       0       16      0.00%
Function Generators  9       512     1.76%
CLB Slices           5       256     1.95%
Dffs or Latches      0       776     0.00%
Block RAMs           0       4       0.00%
Block Multipliers    0       4       0.00%
Block Multiplier Dffs 0      144     0.00%

-----------------------------------------------
```

```
**************************************************

Library: work    Cell: PIPE_CONTROLLER    View: logic

**************************************************

 Cell    Library  References     Total Area

IBUF     xcv2     7 x
LUT1     xcv2     1 x     1     1 Function Generators
LUT2     xcv2     1 x     1     1 Function Generators
LUT3     xcv2     2 x     1     2 Function Generators
LUT4     xcv2     5 x     1     5 Function Generators
MUXF5    xcv2     1 x     1     1 MUXF5
OBUF     xcv2     8 x

Number of ports :                 41
Number of nets :                  32
Number of instances :             25
Number of references to this view :    0

Total accumulated area :
Number of Function Generators :       9
Number of MUXF5 :                     1
Number of gates :                     9
Number of accumulated instances :     25
```

**Timing**

```
            CTE Report Summary

             Clock Frequency Report

                                Domain            Clock Name                  Min Period (Freq)
                                ------            ----------                  ----------------
                                --
                                Design_Clock      Design_Clock                6.495 (153.965 MHz)
End CTE Report Summary ..... CPU Time Used: 0 sec.
          #NAME?
           CTE Report Summary

Analyzing setup constraint violations 10
```

Setup Slack Path Summary

| Index | Setup Slack | Data Path Delay | Source Clock | Dest. Clock | Data End Start Pin | Data End Pin | Edge |
|---|---|---|---|---|---|---|---|
| 1 | 3.505 | 6.495 | Design_Clock | Design_Clock | INSTRUCTION(27) | ALUSrcB | Fall |
| 2 | 3.505 | 6.495 | Design_Clock | Design_Clock | INSTRUCTION(26) | ALUSrcB | Fall |
| 3 | 3.682 | 6.318 | Design_Clock | Design_Clock | INSTRUCTION(28) | ALUSrcB | Fall |
| 4 | 3.821 | 6.179 | Design_Clock | Design_Clock | INSTRUCTION(29) | ALUSrcB | Rise |
| 5 | 3.821 | 6.179 | Design_Clock | Design_Clock | INSTRUCTION(31) | ALUSrcB | Rise |
| 6 | 3.821 | 6.179 | Design_Clock | Design_Clock | INSTRUCTION(30) | ALUSrcB | Fall |
| 7 | 5.446 | 4.554 | Design_Clock | Design_Clock | HAZARD | HAZARD_CTRL | Rise |

End CTE Report Summary ..... CPU Time Used: 0 sec.

#NAME?

CTE Critical Path Report

-- CTE get true worst setup path..

Critical path #1, (path slack = 3.51):

SOURCE CLOCK: name: Design_Clock period: 10.000000

Times are relative to the 1st rising edge

DEST CLOCK: name: Design_Clock period: 10.000000

Times are relative to the 2nd rising edge

| NAME | GATE | DELAY | ARRIVAL | DIR | FANOUT |
|---|---|---|---|---|---|
| INSTRUCTION(27) | (port) | | 0.00 | dn | |
| INSTRUCTION(27) | (net) | 0.00 | | | 1 |
| INSTRUCTION_ibuf(27)/I | IBUF(LVTTL) | | 0.00 | dn | |
| INSTRUCTION_ibuf(27)/O | IBUF(LVTTL) | 0.95 | 0.95 | dn | |
| INSTRUCTION_int(27) | (net) | 0.00 | | | 3 |
| i23e8x2/I0 | LUT2 | | 0.95 | dn | |
| i23e8x2/O | LUT2 | 0.49 | 1.44 | up | |
| n23e8x2 | (net) | 0.00 | | | 1 |
| i23e8x1/S | MUXF5 | | 1.44 | up | |
| i23e8x1/O | MUXF5 | 0.83 | 2.27 | up | |
| n23e8x1 | (net) | 0.00 | | | 3 |
| i6197x1/I0 | LUT1 | | 2.27 | up | |
| i6197x1/O | LUT1 | 0.49 | 2.75 | dn | |
| ALUSrcB_dup0 | (net) | 0.00 | | | 1 |
| ALUSrcB_obuf/I | OBUF(LVTTL,SLOW,12) | | 2.75 | dn | |

ALUSrcB_obuf/O OBUF(LVTTL,SLOW,12) 3.74 6.49 dn
ALUSrcB (net) 0.00 0
ALUSrcB (port) 6.49 dn

Initial edge separation: 10.00
Source clock delay: - 0.00
Dest clock delay: + 0.00
---
Edge separation: 10.00
Setup constraint: - 0.00
---
Data required time: 10.00
Data arrival time: - 6.49
---
Slack: 3.51

-- CPU Time Used: 0 sec.
End CTE Analysis ..... CPU Time Used: 0 sec.

## IF Stage

### Hardware

**********
Device Utilization for 2V40cs144
**********

| Resource | Used | Avail | Utilization |
|---|---|---|---|
| IOs | 34 | 88 | 38.64% |
| Global Buffers | 1 | 16 | 6.25% |
| Function Generators | 13 | 512 | 2.54% |
| CLB Slices | 18 | 256 | 7.03% |
| Dffs or Latches | 36 | 776 | 4.64% |
| Block RAMs | 0 | 4 | 0.00% |
| Block Multipliers | 0 | 4 | 0.00% |
| Block Multiplier Dffs | 0 | 144 | 0.00% |

---

**********

Library: work Cell: IF_STAGE View: logic

```
**********************************************

 Cell              Library  References     Total Area

 BUFGP              xcv2        1 x
 FDR                xcv2        6 x     1     6 Dffs or Latches
 FDRE               xcv2        1 x     1     1 Dffs or Latches
 GND                xcv2        1 x
 IBUF               xcv2        2 x
 LUT1               xcv2        2 x     1     2 Function Generators
 LUT2               xcv2        1 x     1     1 Function Generators
 LUT4               xcv2       10 x     1    10 Function Generators
 OBUF               xcv2       32 x
 modgen_counter_29_0   OPERATORS     1 x     28     28 MUX
CARRYs
                              29     29 Dffs or Latches

 Number of ports :                 35
 Number of nets :                  88
 Number of instances :             57
 Number of references to this view :    0

Total accumulated area :
 Number of Dffs or Latches :          36
 Number of Function Generators :      13
 Number of MUX CARRYs :               28
 Number of gates :                    13
 Number of accumulated instances :    144
```

**Timing**

| Index | Setup Slack | Data Path Delay | Source Clock | Dest. Clock | Data Start Pin | Data End Pin | Data End Edge |
|---|---|---|---|---|---|---|---|
| 1 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)/C | INSTRUCTION(0) | Rise |
| 2 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)_repl5/C | INSTRUCTION(16) | Rise |
| 3 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)_repl4/C | INSTRUCTION(12) | Rise |
| 4 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)_repl3/C | INSTRUCTION(5) | Rise |
| 5 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)_repl2/C | INSTRUCTION(3) | Rise |
| 6 | 4.462 | 4.331 | CLK | CLK | reg_INSTRUCTION(0)_repl1/C | INSTRUCTION(2) | Rise |
| 7 | 5.944 | 3.763 | CLK | CLK | reg_PC(2)/C | modgen_counter_PC/reg_q(31)/D | Rise |
| 8 | 6.551 | 3.156 | CLK | CLK | modgen_counter_PC/reg_q(3)/C | modgen_counter_PC/reg_q(31)/D | Rise |

```
 9   6.634  3.073  CLK    CLK   modgen_counter_PC/reg_q(4)/C  modgen_counter_PC/reg_q(31)/D  Rise
10   6.675  3.032  CLK    CLK   modgen_counter_PC/reg_q(5)/C  modgen_counter_PC/reg_q(31)/D  Rise

End CTE Report Summary ..... CPU Time Used: 0 sec.
                            #NAME?
                    CTE Critical Path Report
-- CTE get true worst setup path..


Critical path #1, (path slack = 4.46):

SOURCE CLOCK: name: CLK period: 10.000000
    Times are relative to the 1st rising edge
  DEST CLOCK: name: CLK period: 10.000000
    Times are relative to the 2nd rising edge

NAME                  GATE              DELAY    ARRIVAL DIR  FANOUT
reg_INSTRUCTION(0)/C  FDR                          0.00   up
reg_INSTRUCTION(0)/Q  FDR                  0.59    0.59   up
INSTRUCTION_dup0(0)   (net)                0.00           1
INSTRUCTION_obuf(0)/I OBUF(LVTTL,SLOW,12)             0.59   up
INSTRUCTION_obuf(0)/O OBUF(LVTTL,SLOW,12)      3.74    4.33   up
INSTRUCTION(0)        (net)                0.00           0
INSTRUCTION(0)        (port)                      4.33   up

                                                  Initial edge separation:     10.00
                                                  Source clock delay:     -
                                                  1.21
                                                  Dest clock delay:       +
                                                  0.00
                                                               ----------
                                                  Edge separation:
                                                  8.79
                                                  Setup constraint:       -
                                                  0.00
                                                               ----------
                                                  Data required time:
                                                  8.79
                                                  Data arrival time:      -
                                                  4.33
                                                               ----------
                                                  Slack:                  4.46

-- CPU Time Used: 0 sec.
```

End CTE Analysis ..... CPU Time Used: 0 sec.

## EX Stage

### Hardware

```
**********************************************
Device Utilization for 2V40cs144
**********************************************
Resource             Used    Avail   Utilization
-----------------------------------------------
IOs                  259     88      294.32%
Global Buffers       0       16      0.00%
Function Generators  1526    512     298.05%
CLB Slices           763     256     298.05%
Dffs or Latches      0       776     0.00%
Block RAMs           0       4       0.00%
Block Multipliers    0       4       0.00%
Block Multiplier Dffs  0     144     0.00%

-----------------------------------------------
WARNING: This design does not fit in the device specified!
Recommending to try an alternate device ...
**********************************************
Device Utilization for 2V500fg456
**********************************************
Resource             Used    Avail   Utilization
-----------------------------------------------
IOs                  259     264     98.11%
Global Buffers       0       16      0.00%
Function Generators  1526    6144    24.84%
CLB Slices           763     3072    24.84%
Dffs or Latches      0       6936    0.00%
Block RAMs           0       32      0.00%
Block Multipliers    0       32      0.00%
Block Multiplier Dffs  0     1152    0.00%

-----------------------------------------------

*************************************************

Library: work    Cell: EX_STAGE    View: implementation
```

**********

| Cell | Library | References | Total Area |
|---|---|---|---|
| GND | xcv2 | 1 x | |
| IBUF | xcv2 | 175 x | |
| LUT2 | xcv2 | 11 x 1 | 11 Function Generators |
| LUT3 | xcv2 | 555 x 1 | 555 Function Generators |
| LUT4 | xcv2 | 704 x 1 | 704 Function Generators |
| LUT4_L | xcv2 | 256 x 1 | 256 Function Generators |
| MUXCY_L | xcv2 | 252 x 1 | 252 MUX CARRYs |
| MUXF5 | xcv2 | 62 x 1 | 62 MUXF5 |
| MUXF6 | xcv2 | 24 x 1 | 24 MUXF6 |
| OBUF | xcv2 | 64 x | |
| VCC | xcv2 | 1 x | |
| XORCY | xcv2 | 256 x | |

Number of ports : 259
Number of nets : 2536
Number of instances : 2361
Number of references to this view : 0

Total accumulated area :
Number of Function Generators : 1526
Number of MUX CARRYs : 252
Number of MUXF5 : 62
Number of MUXF6 : 24
Number of gates : 1522
Number of accumulated instances : 2361

## Timing

CTE Report Summary

Clock Frequency Report

| Domain | Clock Name | Min Period (Freq) |
|---|---|---|
| Design_Clock | Design_Clock | 9.027 (110.779 MHz) |

End CTE Report Summary ..... CPU Time Used: 1 sec.
#NAME?

CTE Report Summary

Analyzing setup constraint violations 10

Setup Slack Path Summary

| Index | Setup Slack | Path Delay | Source Clock | Dest. Clock | Data Start Pin | Data End Pin | Edge |
|---|---|---|---|---|---|---|---|
| 1 | 0.973 | 9.027 | Design_Clock | Design_Clock | ALUSrcB_p | ALUOuput_p(3) | Fall |
| 2 | 1.669 | 8.331 | Design_Clock | Design_Clock | B_p(16) | ALUOuput_p(3) | Fall |
| 3 | 1.669 | 8.331 | Design_Clock | Design_Clock | Imm_p(16) | ALUOuput_p(3) | Rise |
| 4 | 1.669 | 8.331 | Design_Clock | Design_Clock | B_p(19) | ALUOuput_p(3) | Rise |
| 5 | 1.669 | 8.331 | Design_Clock | Design_Clock | Imm_p(23) | ALUOuput_p(3) | Fall |
| 6 | 1.669 | 8.331 | Design_Clock | Design_Clock | Imm_p(25) | ALUOuput_p(3) | Fall |
| 7 | 1.669 | 8.331 | Design_Clock | Design_Clock | Imm_p(26) | ALUOuput_p(3) | Rise |
| 8 | 1.669 | 8.331 | Design_Clock | Design_Clock | Imm_p(24) | ALUOuput_p(3) | Fall |
| 9 | 1.669 | 8.331 | Design_Clock | Design_Clock | B_p(17) | ALUOuput_p(3) | Fall |
| 10 | 1.669 | 8.331 | Design_Clock | Design_Clock | B_p(25) | ALUOuput_p(3) | Rise |

End CTE Report Summary ..... CPU Time Used: 0 sec.

#NAME?

CTE Critical Path Report

-- CTE get true worst setup path..

Critical path #1, (path slack = 0.97):

SOURCE CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 1st rising edge
DEST CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 2nd rising edge

| NAME | GATE | DELAY | ARRIVAL | DIR | FANOUT |
|---|---|---|---|---|---|
| ALUSrcB_p | (port) | | 0.00 | dn | |
| ALUSrcB_p | (net) | 0.00 | | | 1 |
| ALUSrcB_p_ibuf/I | IBUF(LVTTL) | | 0.00 | dn | |
| ALUSrcB_p_ibuf/O | IBUF(LVTTL) | 1.51 | 1.51 | dn | |
| ALUSrcB_p_int | (net) | 0.00 | | | 389 |
| i9dbdx212/I0 | LUT3 | | 1.51 | dn | |
| i9dbdx212/O | LUT3 | 0.63 | 2.13 | up | |
| ALUin2_s(16) | (net) | 0.00 | | | 4 |

i9dbdx211/I0 LUT4 2.13 up
i9dbdx211/O LUT4 0.49 2.62 up
n9dbdx197 (net) 0.00 1
i9dbdx203/I3 LUT4 2.62 up
i9dbdx203/O LUT4 0.63 3.24 up
NOT_a(1)_dup_12648 (net) 0.00 2
i2612x15/I2 LUT4 3.24 up
i2612x15/O LUT4 0.63 3.87 up
n2612x13 (net) 0.00 3
i2612x14/I1 LUT4 3.87 up
i2612x14/O LUT4 0.76 4.63 up
n2612x12 (net) 0.00 18
i6c30x16/I3 LUT4 4.63 up
i6c30x16/O LUT4 0.63 5.26 up
n6c30x12 (net) 0.00 15
ie059x11/I2 LUT3 5.26 up
ie059x11/O LUT3 0.63 5.88 up
ne059x9 (net) 0.00 4
ie059x10/I3 LUT4 5.88 up
ie059x10/O LUT4 0.49 6.37 dn
ne059x8 (net) 0.00 1
ie059x5/I3 LUT4 6.37 dn
ie059x5/O LUT4 0.49 6.86 dn
ne059x3 (net) 0.00 1
ie059x2/I3 LUT4 6.86 dn
ie059x2/O LUT4 0.49 7.34 dn
ne059x1 (net) 0.00 1
ie059x1/I0 LUT4 7.34 dn
ie059x1/O LUT4 0.49 7.83 dn
ALUOuput_p_dup0(3) (net) 0.00 1
ALUOuput_p_obuf(3)/I OBUF(LVTTL,FAST,24) 7.83 dn
ALUOuput_p_obuf(3)/O OBUF(LVTTL,FAST,24) 1.20 9.03 dn
ALUOuput_p(3) (net) 0.00 0
ALUOuput_p(3) (port) 9.03 dn

Initial edge separation: 10.00
Source clock delay: - 0.00
Dest clock delay: + 0.00
---
Edge separation: 10.00
Setup constraint: - 0.00
---
Data required time: 10.00

Data arrival time: - 9.03

---

Slack: 0.97

-- CPU Time Used: 0 sec.
End CTE Analysis ..... CPU Time Used: 0 sec.

## ID/WEB Stage

### Hardware

**********
Device Utilization for 2V40cs144
**********
Resource Used Avail Utilization
---
IOs 328 88 372.73%
Global Buffers 0 16 0.00%
Function Generators 2284 512 446.09%
CLB Slices 1142 256 446.09%
Dffs or Latches 1984 776
255.67%
Block RAMs 0 4 0.00%
Block Multipliers 0 4 0.00%
Block Multiplier Dffs 0 144
0.00%

---
WARNING: This design does not fit in the device specified!
Recommending to try an alternate device ...
**********
Device Utilization for 2V1000bg575
**********
Resource Used Avail Utilization
---
IOs 328 328 100.00%
Global Buffers 0 16 0.00%
Function Generators 2284 10240 22.30%
CLB Slices 1142 5120 22.30%
Dffs or Latches 1984 11224
17.68%
Block RAMs 0 40 0.00%
Block Multipliers 0 40 0.00%

Block Multiplier Dffs 0 1440
0.00%

---

**********

Library: work Cell: ID_WB_STAGE View: logic

**********

| Cell | Library | References | Total Area |
|---|---|---|---|
| GND | xcv2 | 1 x | |
| IBUF | xcv2 | 163 x | |
| LDC | xcv2 | 1975 x 1 | 1975 Dffs or Latches |
| LDP | xcv2 | 9 x 1 | 9 Dffs or Latches |
| LUT2 | xcv2 | 136 x 1 | 136 Function Generators |
| LUT3 | xcv2 | 2117 x 1 | 2117 Function Generators |
| LUT4 | xcv2 | 31 x 1 | 31 Function Generators |
| MUXF5 | xcv2 | 1024 x 1 | 1024 MUXF5 |
| MUXF6 | xcv2 | 512 x 1 | 512 MUXF6 |
| MUXF7 | xcv2 | 256 x 1 | 256 MUXF7 |
| MUXF8 | xcv2 | 128 x 1 | 128 MUXF8 |
| OBUF | xcv2 | 165 x | |

Number of ports : 328
Number of nets : 6680
Number of instances : 6517
Number of references to this view : 0

Total accumulated area :
Number of Dffs or Latches : 1984
Number of Function Generators : 2284
Number of MUXF5 : 1024
Number of MUXF6 : 512
Number of MUXF7 : 256
Number of MUXF8 : 128

Number of gates : 2284
Number of accumulated instances : 6517

**Timing**

CTE Report Summary

Clock Frequency Report

| Domain | Clock Name | Min Period (Freq) |
|---|---|---|
| Design_Clock | Design_Clock | 5.736 (174.338 MHz) |

End CTE Report Summary ..... CPU Time Used: 1 sec.
#NAME?
CTE Report Summary

Analyzing setup constraint violations 10

Setup Slack Path Summary

| Index | Setup Slack | Data Path Delay | Source Clock | Dest. Clock | Data Start Pin | Data End Pin | Data End Edge |
|---|---|---|---|---|---|---|---|
| 1 | 4.264 | 5.736 | Design_Clock | Design_Clock | Instruction(20) | WriteReg_OUT(4) | Fall |
| 2 | 4.264 | 5.736 | Design_Clock | Design_Clock | Instruction(16) | WriteReg_OUT(0) | Rise |
| 3 | 4.264 | 5.736 | Design_Clock | Design_Clock | Instruction(19) | WriteReg_OUT(3) | Rise |
| 4 | 4.264 | 5.736 | Design_Clock | Design_Clock | Instruction(18) | WriteReg_OUT(2) | Fall |
| 5 | 4.264 | 5.736 | Design_Clock | Design_Clock | Instruction(17) | WriteReg_OUT(1) | Rise |
| 6 | 4.682 | 5.318 | Design_Clock | Design_Clock | Instruction(15) | WriteReg_OUT(4) | Rise |
| 7 | 4.821 | 5.179 | Design_Clock | Design_Clock | Instruction(14) | WriteReg_OUT(3) | Fall |
| 8 | 4.821 | 5.179 | Design_Clock | Design_Clock | Instruction(12) | WriteReg_OUT(1) | Rise |
| 9 | 4.821 | 5.179 | Design_Clock | Design_Clock | Instruction(11) | WriteReg_OUT(0) | Fall |
| 10 | 4.821 | 5.179 | Design_Clock | Design_Clock | Instruction(13) | WriteReg_OUT(2) | Fall |

End CTE Report Summary ..... CPU Time Used: 0 sec.
#NAME?
CTE Critical Path Report
-- CTE get true worst setup path..

Critical path #1, (path slack = 4.26):

SOURCE CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 1st rising edge
DEST CLOCK: name: Design_Clock period: 10.000000
Times are relative to the 2nd rising edge

| NAME | GATE | DELAY | ARRIVAL | DIR | FANOUT |
|---|---|---|---|---|---|
| Instruction(20) | (port) | | 0.00 | dn | |
| Instruction(20) | (net) | 0.00 | | | 1 |
| Instruction_ibuf(20)/I | IBUF(LVTTL) | | 0.00 | dn | |
| Instruction_ibuf(20)/O | IBUF(LVTTL) | 1.51 | 1.51 | dn | |
| Instruction_int(20) | (net) | 0.00 | | | 65 |
| ic344x1/I2 | LUT3 | | 1.51 | dn | |
| ic344x1/O | LUT3 | 0.49 | 1.99 | dn | |
| WriteReg_OUT_dup0(4) | (net) | 0.00 | | | 1 |
| WriteReg_OUT_obuf(4)/I | OBUF(LVTTL,SLOW,12) | | 1.99 | dn | |
| WriteReg_OUT_obuf(4)/O | OBUF(LVTTL,SLOW,12) | 3.74 | 5.74 | dn | |
| WriteReg_OUT(4) | (net) | 0.00 | | | 0 |
| WriteReg_OUT(4) | (port) | | 5.74 | dn | |

Initial edge separation: 10.00
Source clock delay: - 0.00
Dest clock delay: + 0.00
---
Edge separation: 10.00
Setup constraint: - 0.00
---
Data required time: 10.00
Data arrival time: - 5.74
---
Slack: 4.26

-- CPU Time Used: 0 sec.
End CTE Analysis ..... CPU Time Used: 0 sec.

## MEM Stage

### Hardware

**********
Device Utilization for 2V40cs144
**********

| Resource | Used | Avail | Utilization |
|---|---|---|---|

```
-------------------------------------------
IOs                 194     88      220.45%
Global Buffers      1       16      6.25%
Function Generators 86      512     16.80%
CLB Slices          64      256     25.00%
Dffs or Latches     128     776
16.49%
Block RAMs          0       4       0.00%
Block Multipliers   0       4       0.00%
Block Multiplier Dffs   0       144
0.00%

-------------------------------------------
WARNING: This design does not fit in the device specified!
Recommending to try an alternate device ...
*******************************************
Device Utilization for 2V250fg456
*******************************************
Resource            Used    Avail   Utilization
-------------------------------------------
IOs                 194     200     97.00%
Global Buffers      1       16      6.25%
Function Generators 86      3072    2.80%
CLB Slices          64      1536    4.17%
Dffs or Latches     128     3672
3.49%
Block RAMs          0       24      0.00%
Block Multipliers   0       24      0.00%
Block Multiplier Dffs   0       864
0.00%

-------------------------------------------

*******************************************

Library: work   Cell: MEM_STAGE   View: logic

*******************************************

 Cell   Library  References    Total Area

 BUFGP   xcv2    1
x
 IBUF    xcv2   130
```

x
LDC xcv2 64 x 1 64 Dffs or Latches
LDC_1 xcv2 64 x 1 64 Dffs or Latches
LUT2 xcv2 64 x 1 64 Function Generators
LUT3 xcv2 1 x 1 1 Function Generators
LUT4 xcv2 21 x 1 21 Function Generators
OBUF xcv2 64
x

Number of ports : 195
Number of nets : 540
Number of instances : 409
Number of references to this view : 0

Total accumulated area :
Number of Dffs or Latches : 128
Number of Function Generators :
86
Number of gates : 87
Number of accumulated instances : 409

**Timing**

CTE Report Summary

Clock Frequency Report

| Domain | Clock Name | Min Period (Freq) |
|---|---|---|
| ClockDomain0 | ix3152/out | 1.104 (905.797 MHz) |
| ClockDomain0 | MemRead | 6.624 (150.966 MHz) |

End CTE Report Summary ..... CPU Time Used: 0 sec.
#NAME?
CTE Report Summary

Analyzing setup constraint violations 10

Setup Slack Path Summary

| Index | Setup Slack | Data Path Delay | Source Clock | Dest. Clock | Data Start Pin | Data End Pin | End Edge |
|---|---|---|---|---|---|---|---|

```
----- ----- ----- ------- ------- ----------------- ----------- ----
  1   1.921  1.872  MemRead  MemRead  lat_OUTData(63)/G  OUTData(63)  Rise
  2   1.921  1.872  MemRead  MemRead  lat_OUTData(0)/G   OUTData(0)   Rise
  3   1.921  1.872  MemRead  MemRead  lat_OUTData(2)/G   OUTData(2)   Rise
  4   1.921  1.872  MemRead  MemRead  lat_OUTData(11)/G  OUTData(11)  Rise
  5   1.921  1.872  MemRead  MemRead  lat_OUTData(61)/G  OUTData(61)  Rise
  6   1.921  1.872  MemRead  MemRead  lat_OUTData(10)/G  OUTData(10)  Rise
  7   1.921  1.872  MemRead  MemRead  lat_OUTData(28)/G  OUTData(28)  Rise
  8   1.921  1.872  MemRead  MemRead  lat_OUTData(62)/G  OUTData(62)  Rise
  9   1.921  1.872  MemRead  MemRead  lat_OUTData(1)/G   OUTData(1)   Rise
 10   1.921  1.872  MemRead  MemRead  lat_OUTData(5)/G   OUTData(5)   Rise

End CTE Report Summary ..... CPU Time Used: 0 sec.
            #NAME?
             CTE Critical Path Report
-- CTE get true worst setup path..


Critical path #1, (path slack = 1.92):

SOURCE CLOCK: name: MemRead period: 10.000000
    Times are relative to the 1st falling edge
  DEST CLOCK: name: MemRead period: 10.000000
    Times are relative to the 2nd rising edge

NAME                GATE              DELAY    ARRIVAL DIR  FANOUT
lat_OUTData(63)/G  LDC                        0.00   dn
lat_OUTData(63)/Q  LDC                  0.67     0.67   up
OUTData_dup0(63)   (net)                 0.00              1
OUTData_obuf(63)/I OBUF(LVTTL,FAST,24)              0.67   up
OUTData_obuf(63)/O OBUF(LVTTL,FAST,24)       1.20     1.87   up
OUTData(63)        (net)                 0.00              0
OUTData(63)        (port)                      1.87   up

                                    Initial edge separation:       5.00
                                    Source clock delay:      -     1.21
                                    Dest clock delay:        +     0.00
                                                          ----------
                                    Edge separation:               3.79
                                    Setup constraint:        -     0.00
                                                          ----------
                                    Data required time:            3.79
                                    Data arrival time:       -     1.87
```

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Slack: 1.92