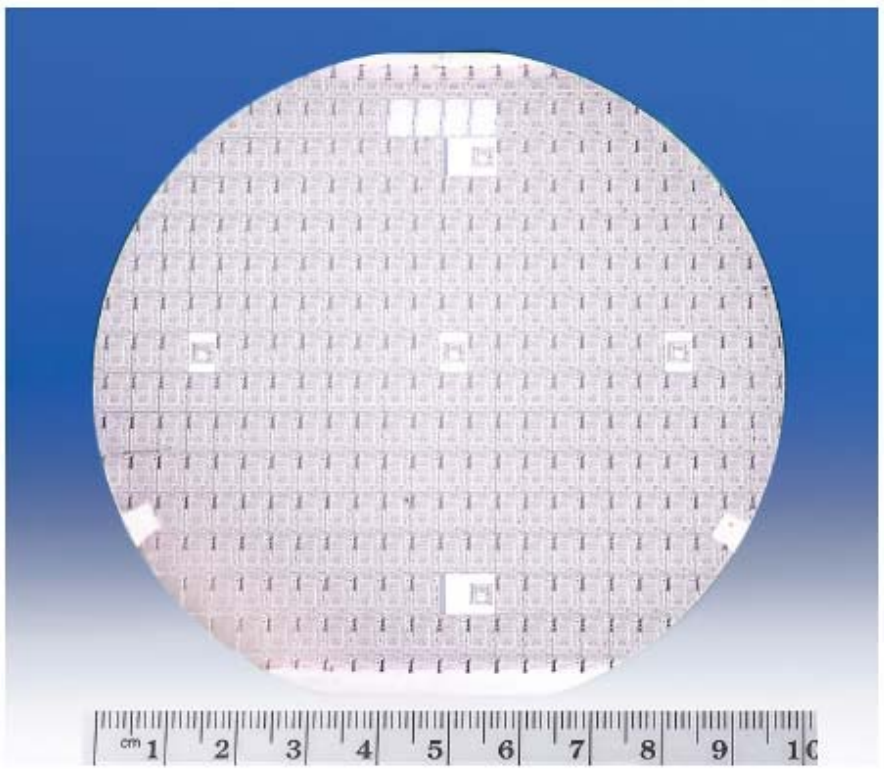
Today's Schedule

- A primer on materials and fabrication of microelectronics BONUS
- Lecture is based on
  - Callister 22.15 - 22.20 (web chapter)
  - Jones, Ch. 4 & Ch. 9
  - Microsystem Engineering of lab-on-a-chip devices, Ch. 6
- ALL of the Ch. 2, 3, 4, 5 and 9 solutions have been placed on WebCT
- Sample of the instruction sheet and attachments also on WebCT
- Wednesday's lecture is a review (study guide)

Si Device Technology



- Hundreds of devices per wafer
- Fabricated in a clean room

Many different techniques for manipulating silicon and silicon-compatible materials have been developed. They can be lumped together into a few general categories:

- substrate fabrication
- optical lithography patterning
- deposition
- etching/removal
- heat treatment
- wafer level packaging

First steps

- Si is very abundant – approximately 27% of the earth's crust
- Generally mined from quartz (SiO_2)
- Reduced to Si using coke: $SiO_2 + 2C \rightarrow Si + 2CO$
- *Metallurgical grade* (MGS)
- Dissolved in HCl to give $SiHCl_3$
- Distilled to give *electronic grade silicon*

- ***Electronic grade silicon*** (EGS) contains about 5 ppm of (Fe, Cr, Mn) and is polycrystalline

Czochralski (CZ) and Float zone (FZ)

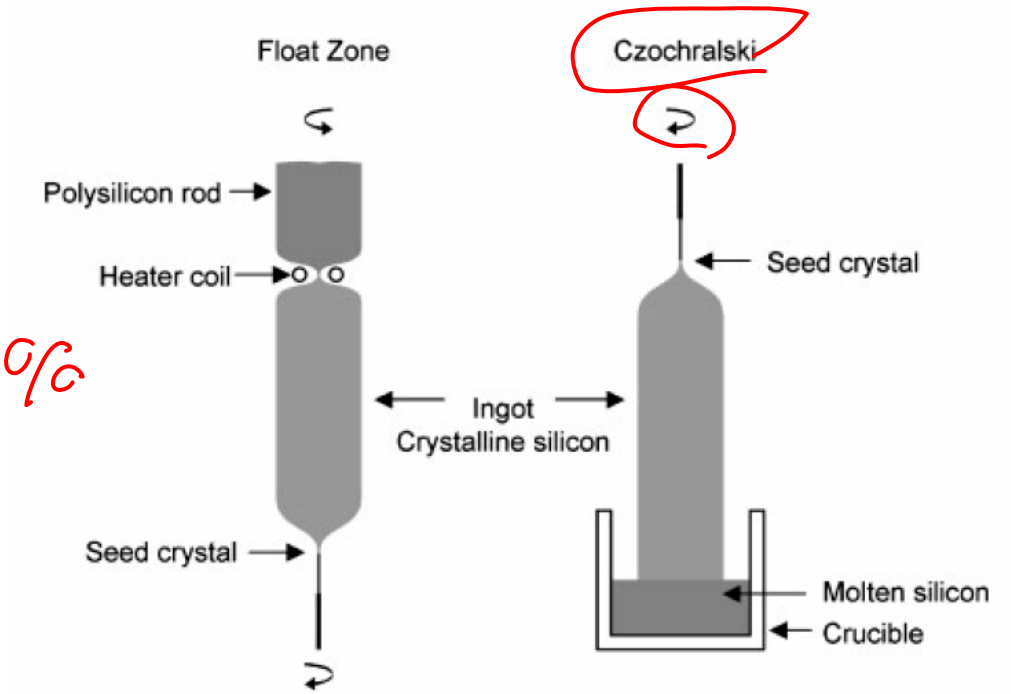


Fig. 6.2 Principle of float-zone and Czochralski crystallization methods.

99.99999%

- CZ contains a lot of oxygen and carbon (due to crucible)
- FZ can be purified over and over. Impurities tend to stay in the *melt*, so they end up at the end of the ingot.
- Dopants to create n or p-type Si can be introduced at either of these stages in the form of impurities in the melt (CZ) or as a gaseous phase (FZ).

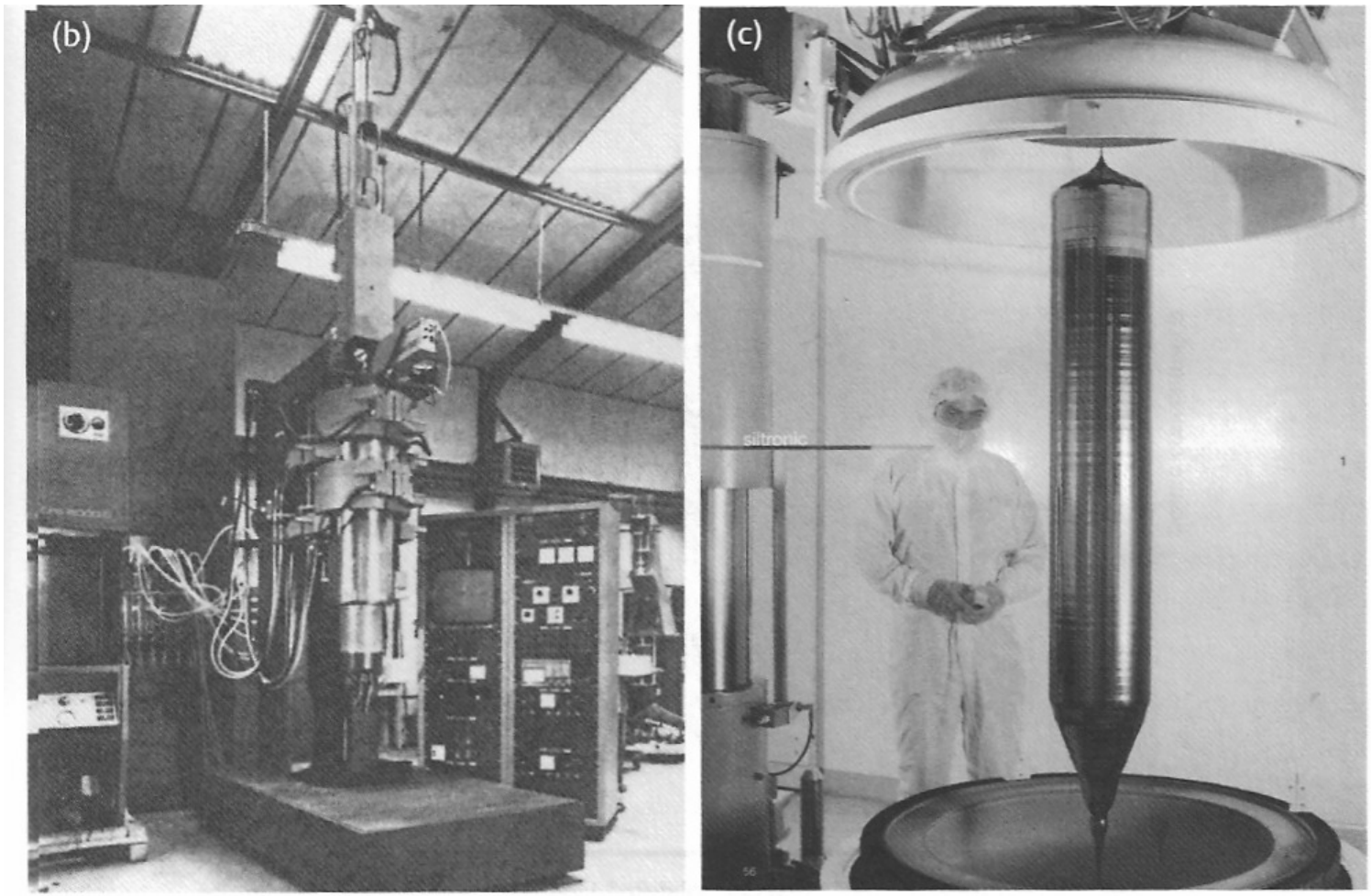
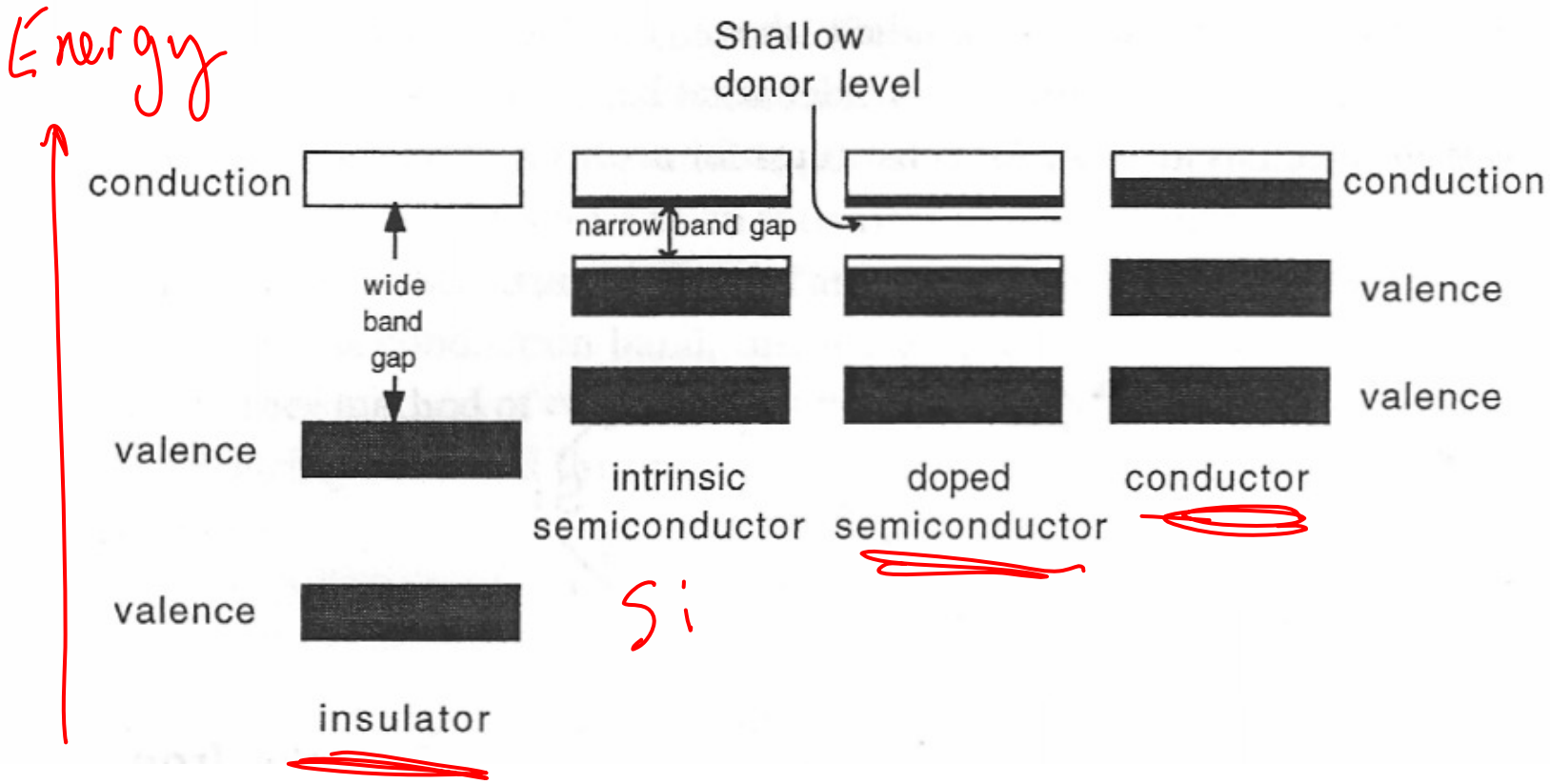


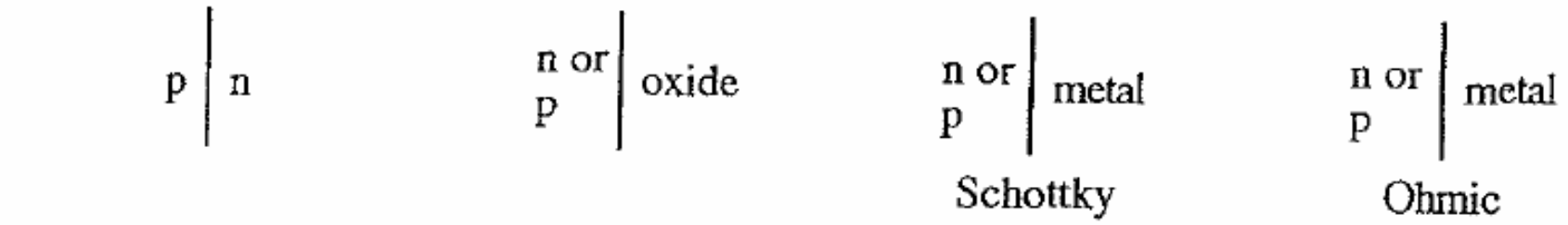
Fig. 9.3 The Czochralski process for growing single crystals of silicon (a) schematic (b) the real thing and (c) a single crystal of silicon, the main part of which contains no dislocations and parts per billion only of harmful impurities. (c) Courtesy of Wacker Siltronic AG, Burghausen, Germany)

Tab. 6.2 Types of specifications for silicon wafers.

Parameter	*Comment*
Wafer material	Silicon (single crystalline)
Growth method	Float zone (FZ) or Czochralski (CZ)
Diameter	Usually mm
Crystal direction	Usually Miller indices are used. Can include a range such as [100] $\pm 1^\circ$
Primary flat	Usually Miller indices are used. Can include a range such as [011] $\pm 1^\circ$
Secondary flat	Often stated as SEMI standard or Miller indices. Can include a range such as $[01\bar{1}] \pm 5^\circ$
Resistivity	Given in Ω cm
Dopant type	p or n type
Dopant	Phosphorous (P) or antimony (As) for n-type Boron (B) for p-type
Thickness	Given in μm and includes a range such as (350 ± 25 μm)
TTV	The difference in thickness between the smallest and the largest thickness of the wafer (best wafers have TTV < 1–2 μm)
Wafer bow	The bending of the wafer (best wafers have bow < 10 μm)


Energy
Shallow
donor level
conduction
narrow band gap
wide
band
gap
valence
valence
conduction
valence
valence
intrinsic
semiconductor
doped
semiconductor
conductor
Si
insulator

Four basic semiconductor interfaces



- **p|n:** rectifying, current flows well in one direction, not in the other
- **(p or n)|oxide:** oxide exerts a field FET
- **(p or n)|metal:** Schottky interface, rectifying
- **(p or n)|metal:** Ohmic interface, non-rectifying

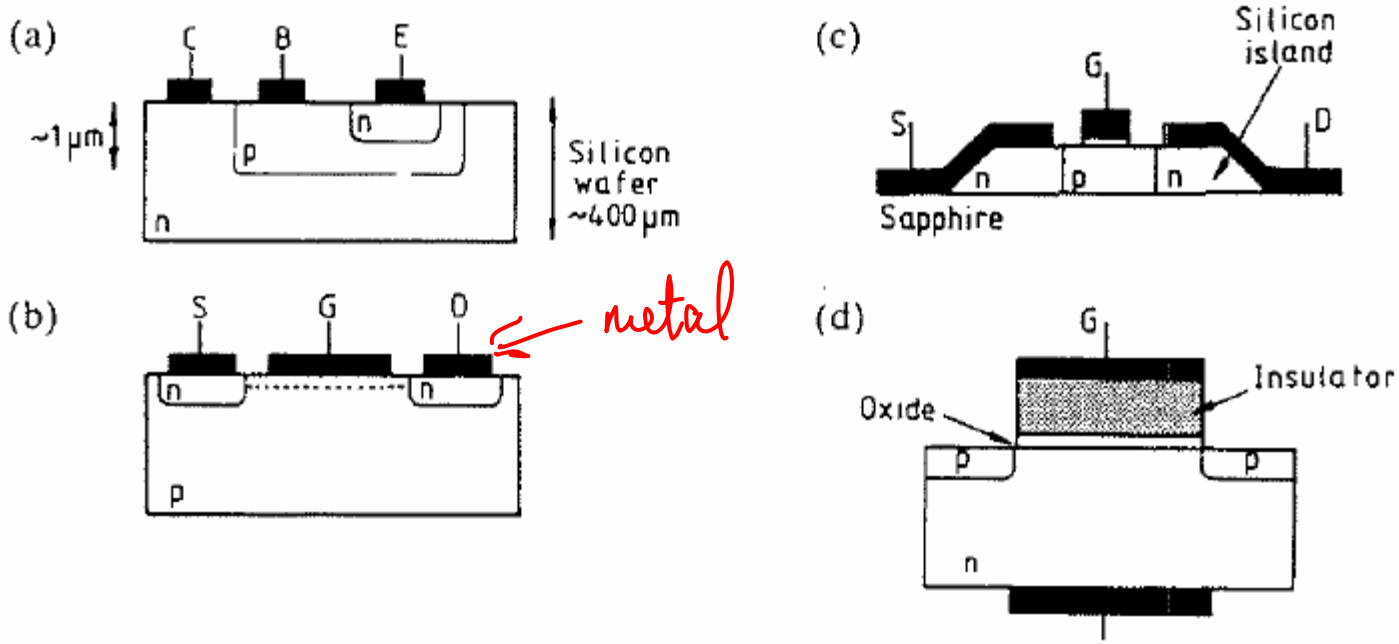


Fig. 9.2 Schematic illustrations of the structure of some simple semiconductor devices: (a) an npn bipolar transistor in a silicon wafer; (b) an n-channel field effect transistor; (c) a silicon-on-insulator field effect transistor; (d) an MIOS memory device (from *Microelectronic materials* by C.R.M. Grovenor, by kind permission of Adam Hilger).

Lithography

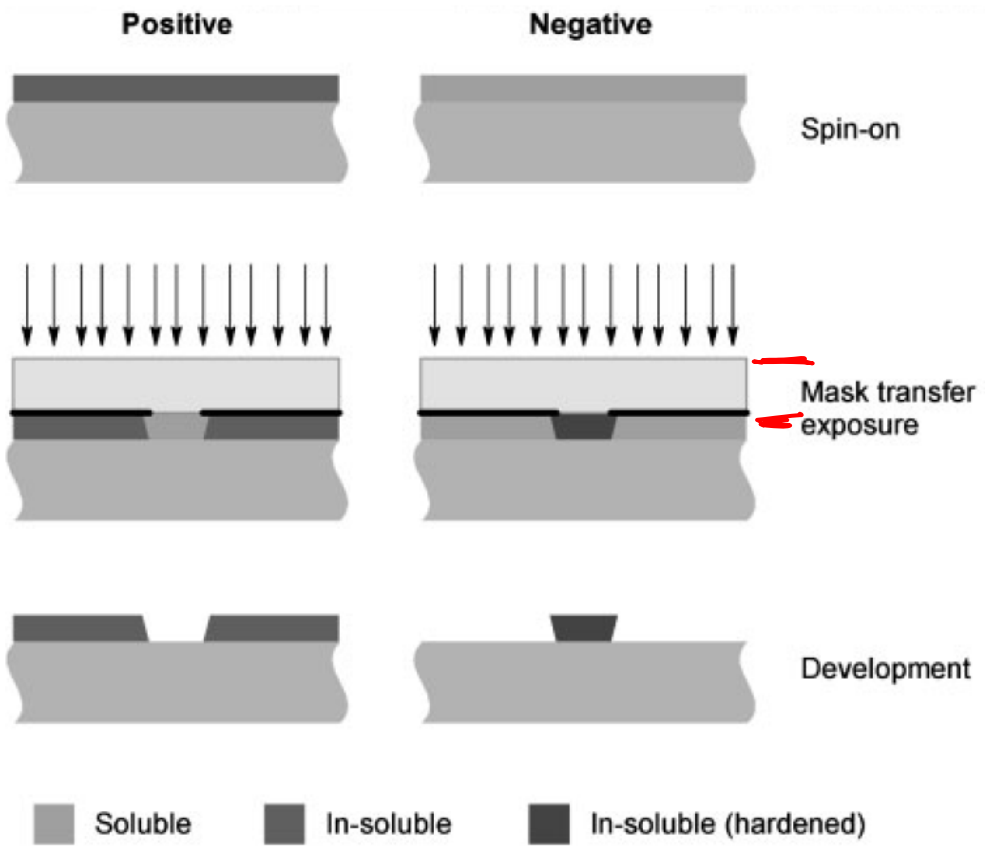
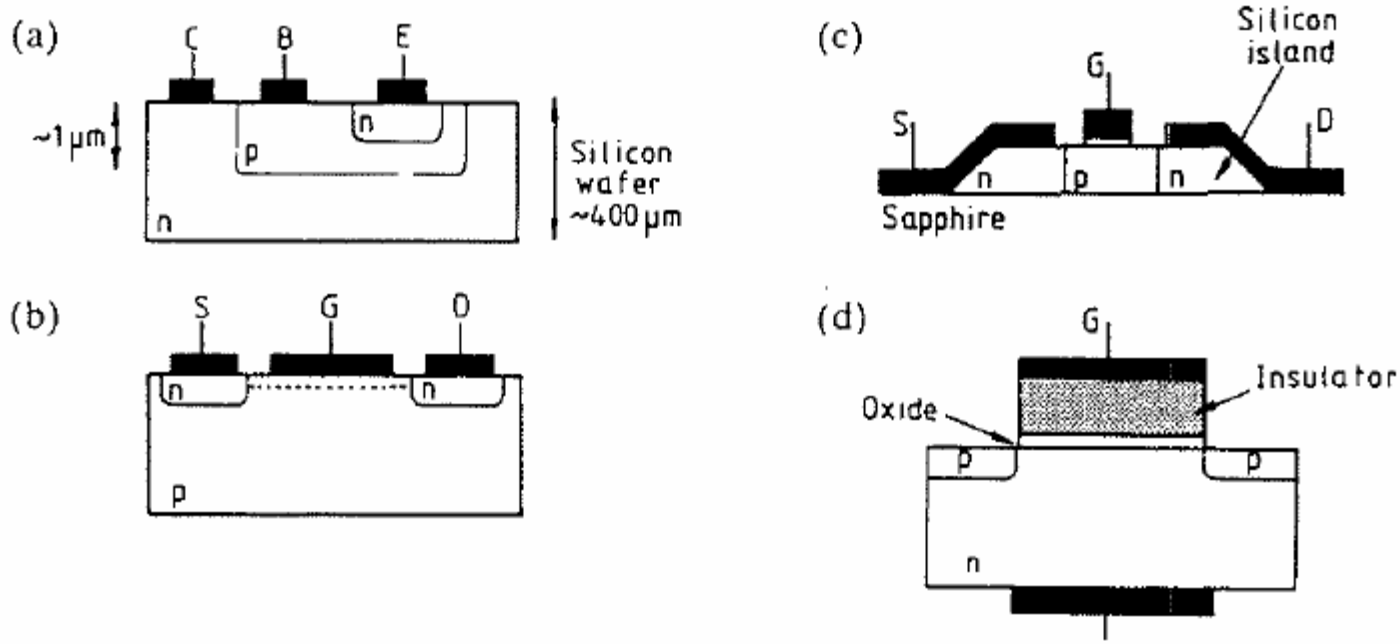


Fig. 6.3 Principle of positive- and negative-tone photoresist.

- Photo-resist is spun-on and masked
- Exposure to UV light either makes it more soluble or less soluble in a developer.
- After development
  - Etch (dry or wet)
  - React (oxidize, dope)
  - Coat (metal, nitride, oxide, other)

Often there are multiple patterning steps to create many levels of the device.



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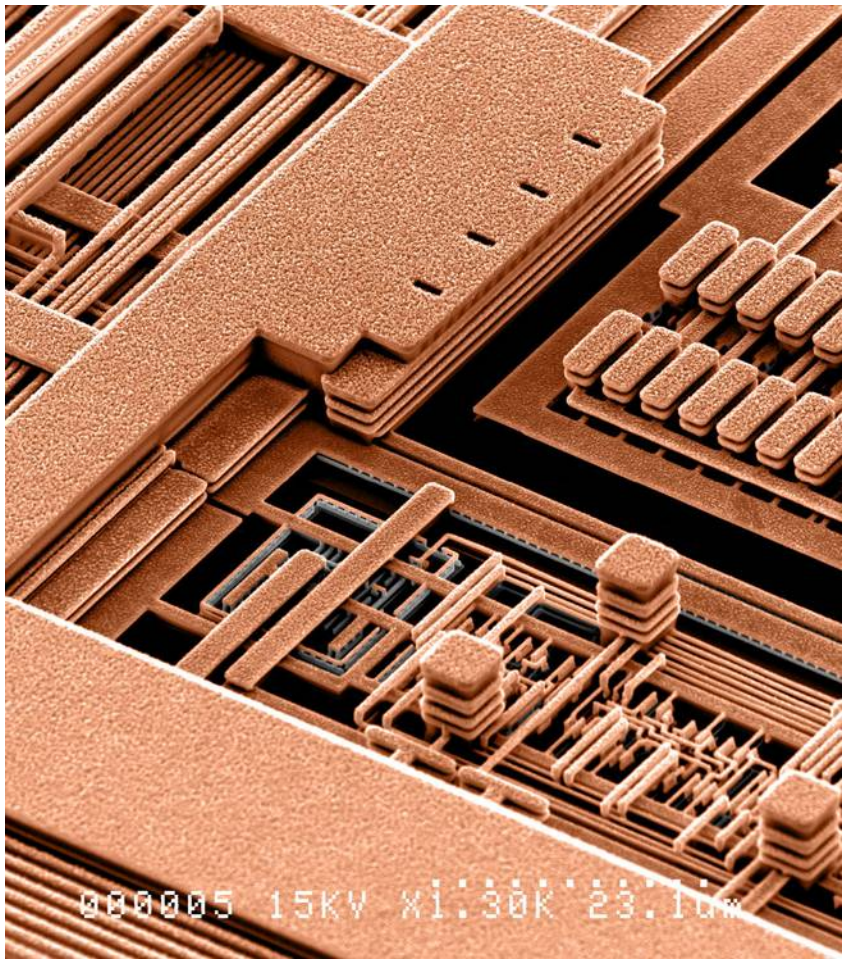
On the chip

- On the chip itself
  - Possibly all 4 types of semiconductor interfaces
  - Complex interconnects (typically Al-1%Si, but increasingly Cu is used)



Chemical Vapor Deposition

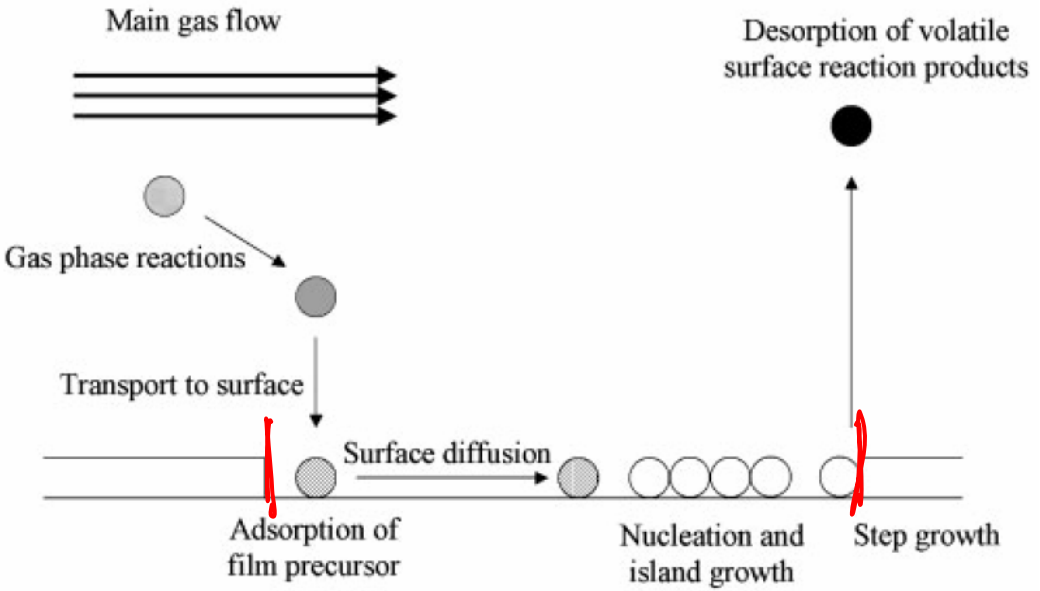


Fig. 6.10 Sketch of the stages involved in chemical vapor deposition (CVD).

$$3\,SiCl_2H_2 + 4\,NH_3 \rightarrow Si_3N_4 + 6\,HCl + 6\,H_2$$

polysilicon
Si
SiO_2
$TiSi_2$
WSi_2

Physical Vapor Deposition

Sputtering

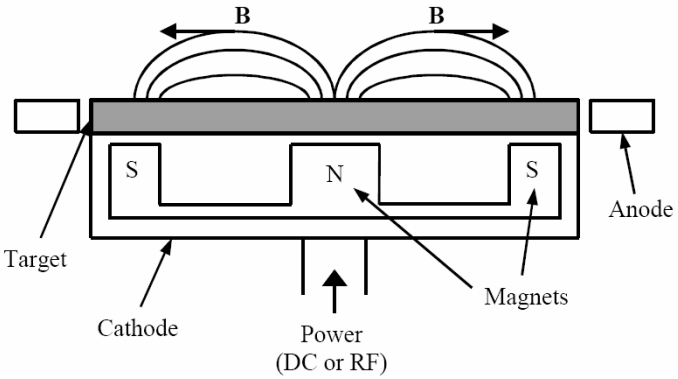
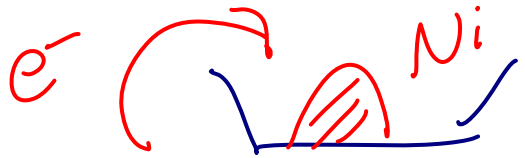
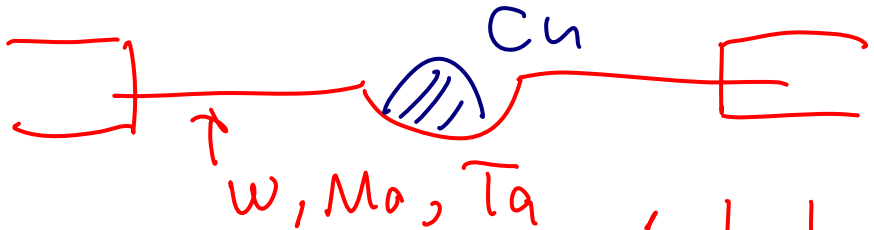


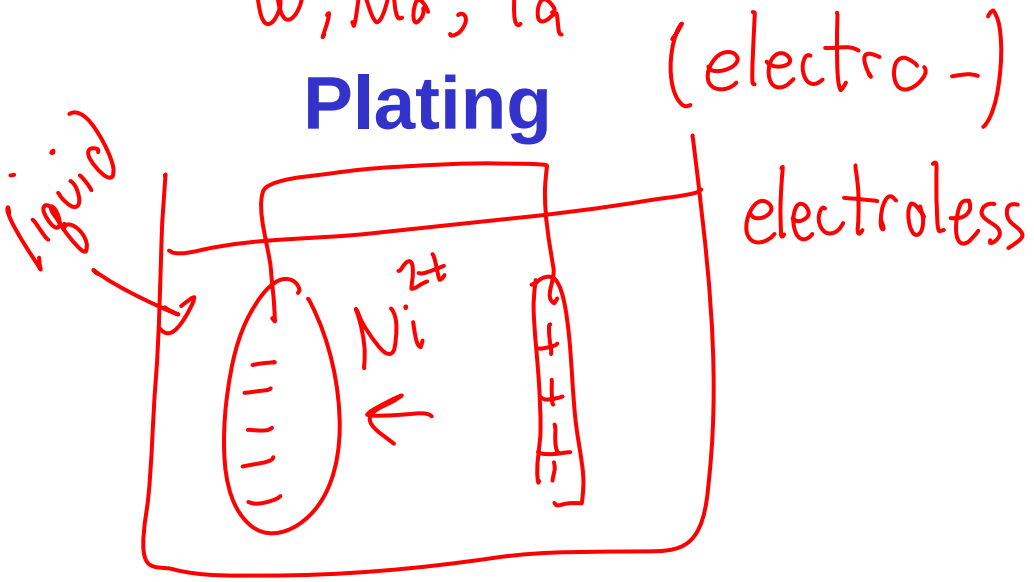
Figure 2.2- A sketch of some of the components of a magnetron sputtering gun.

Evaporation (Thermal and E-beam)





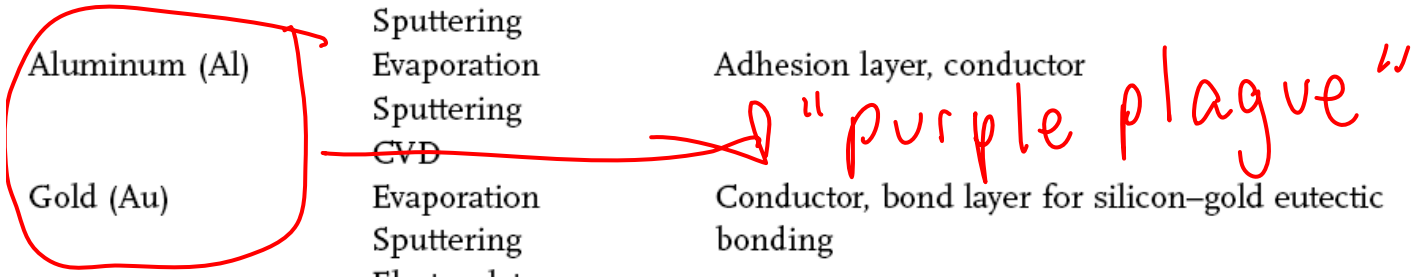
Plating



Physical Vapor Deposition

Tab. 6.3 Various metals often used for microfabrication.

Metal	*Deposition method*	*Use*
Titanium (Ti)	Evaporation Sputtering	Adhesion layer, silicide former
Chromium (Cr)	Evaporation Sputtering	Adhesion layer
Aluminum (Al)	Evaporation Sputtering ~~CVD~~	Adhesion layer, conductor
Gold (Au)	Evaporation Sputtering Electroplate	Conductor, bond layer for silicon–gold eutectic bonding
Platinum (Pt)	Evaporation Sputtering	Conductor, diffusion barrier for gold, often used as electrode in biochemical microsystems
Palladium (Pd)	Evaporation Sputtering	Diffusion barrier for silver, can adsorb large amounts of hydrogen, silicide former
Silver (Ag)	Evaporation Sputtering Electroplate	Conductor, often used as electrode, needed for Ag/AgCl electrode systems
Copper (Cu)	Evaporation Sputtering Electroplate	Conductor, diffuses fast in silicon
Nickel (Ni)	Evaporation Sputtering Electroplate	Conductor, structural material often used for electroplated metal microstructures

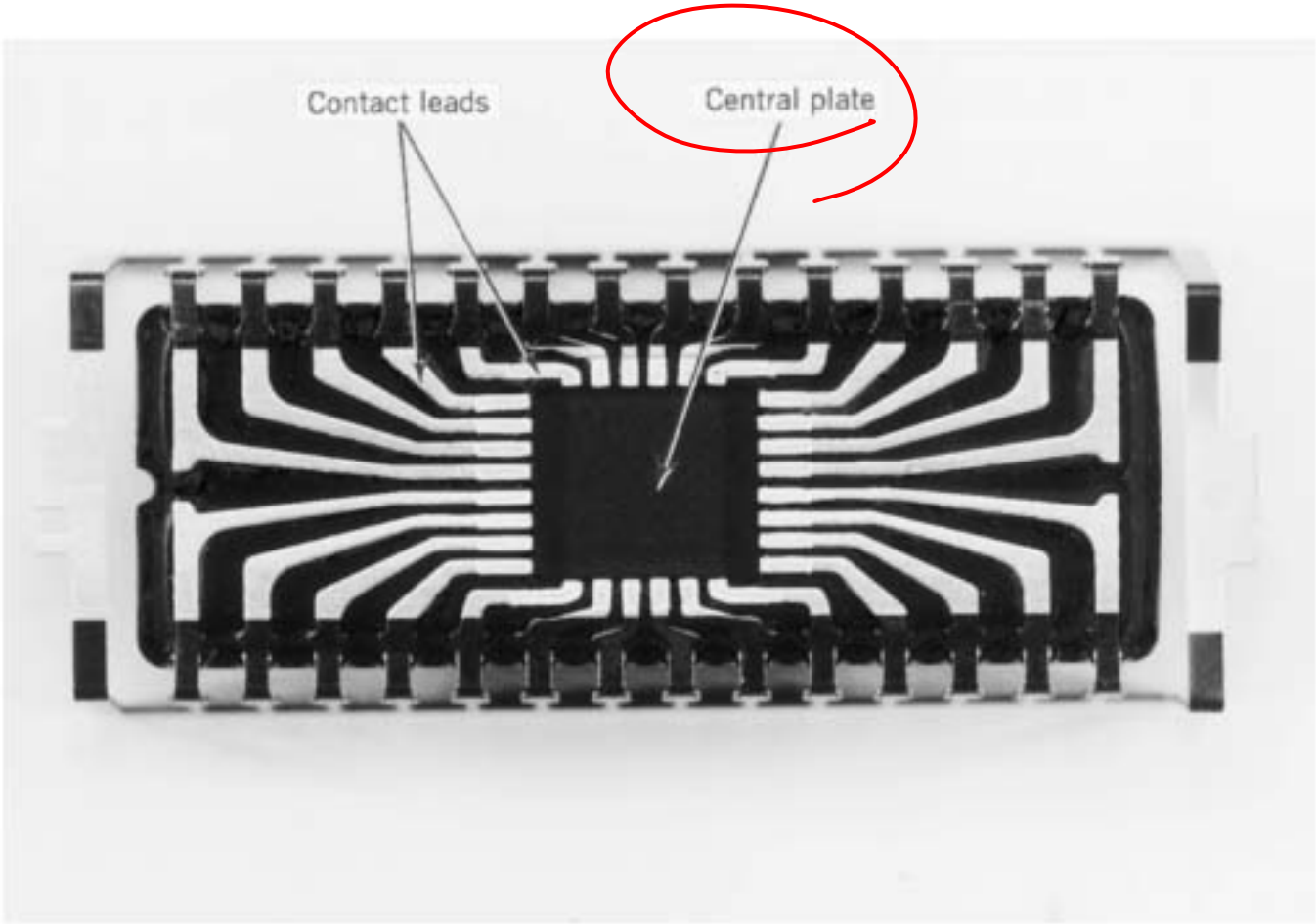


Now the chip must be packaged!

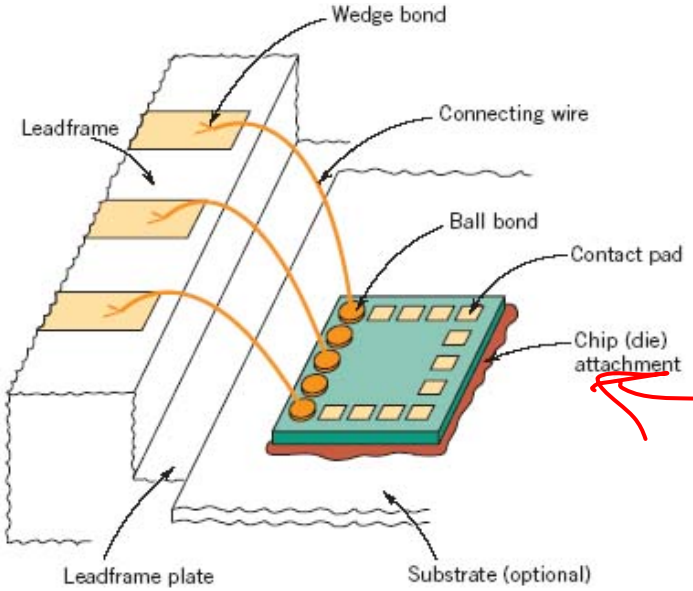
Some of the functions that an integrated circuit package must perform include the following:

1. To permit electrical contact between the devices on the chip and the macroscopic world. The contact pads on the surface of the IC are so minuscule and numerous that accommodation of macroscopic wiring is simply not possible.
2. To dissipate excess heat. While in operation, the many electronic devices generate significant quantities of heat, which must be dissipated away from the chip.
3. To protect delicate electrical connections on the chip from chemical degradation and contamination.
4. To provide mechanical support so that the small and fragile chip may be handled.
5. To provide an adequate electrical interface such that the performance of the IC itself is not significantly degraded by the package design.

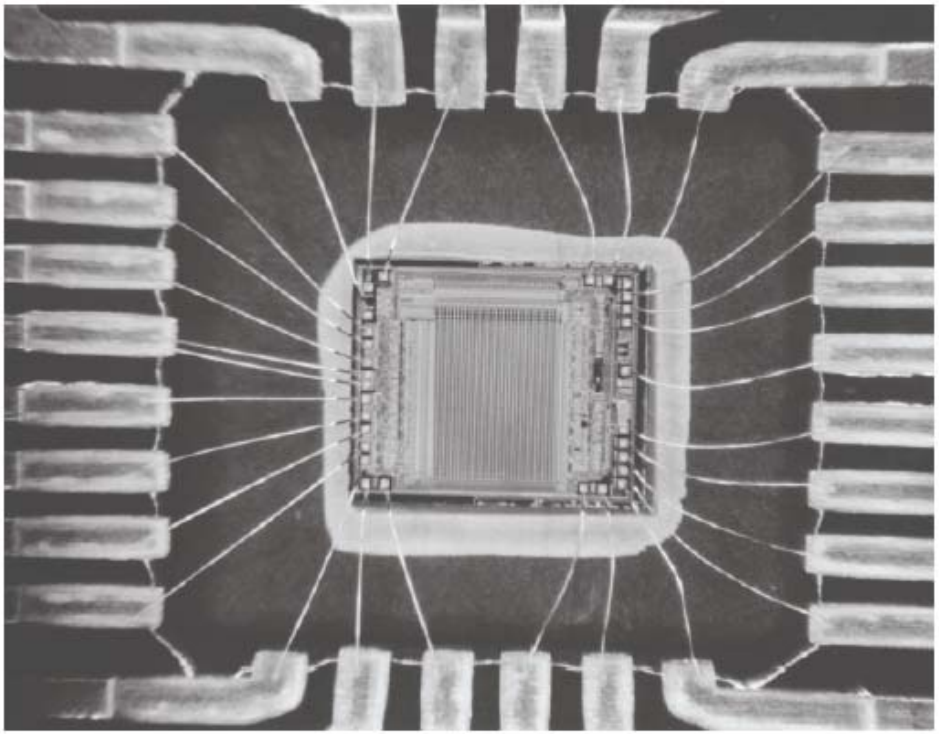
Leadframe



Leadframe



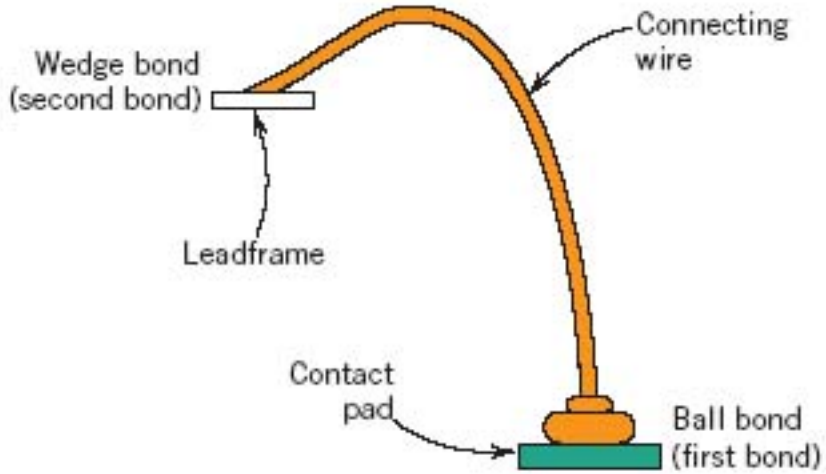
(a)

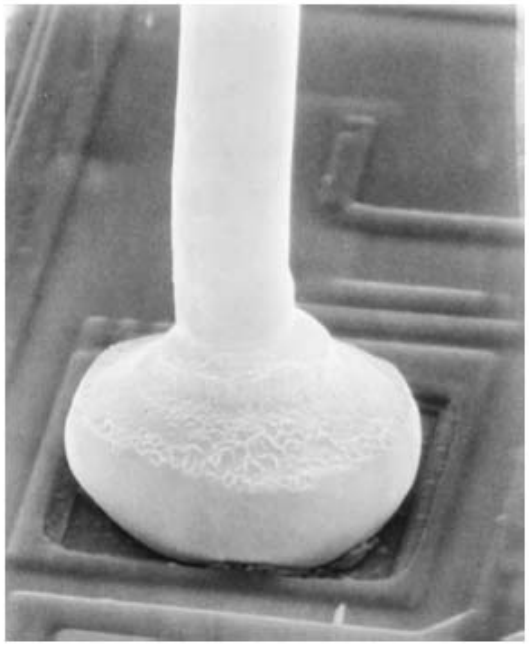


(b)

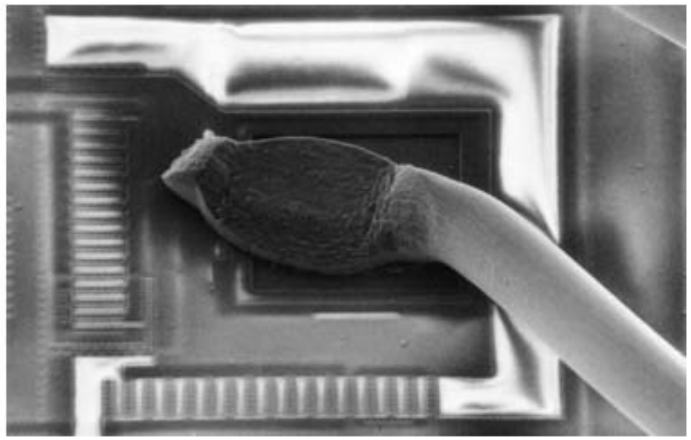
- Bonding of chip to plate either by thermally conductive epoxy (Ag particles) or with Au-Si eutectic solder
- Leads are sometimes Au, but also Cu and Al.
- Automated process

Leadframe



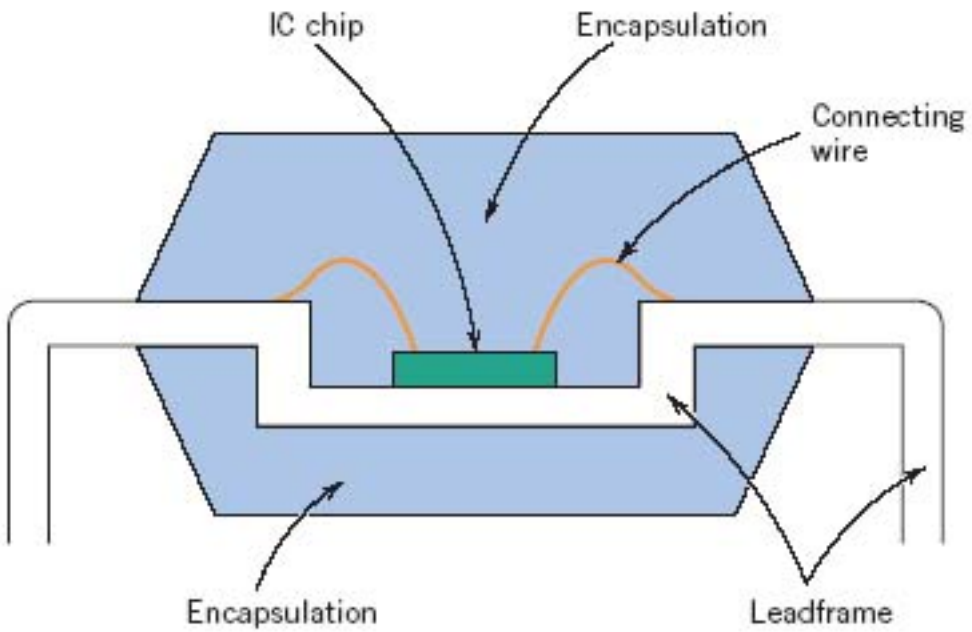


(a)

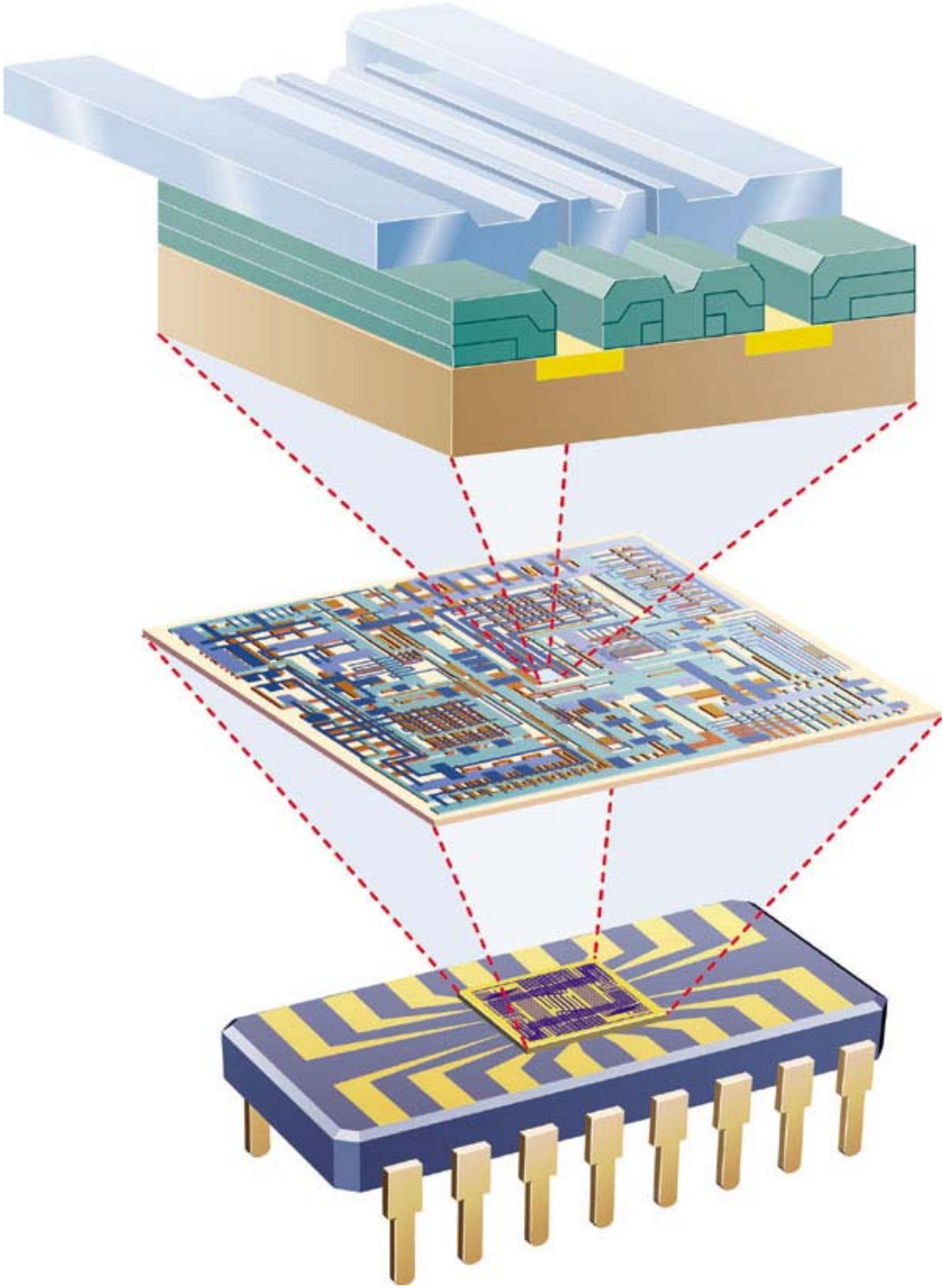


(b)

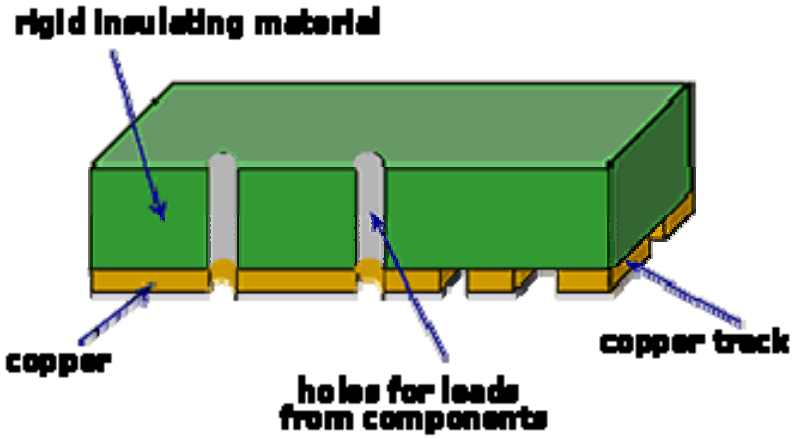
Leadframe


IC chip
Encapsulation
Connecting wire
Encapsulation
Leadframe

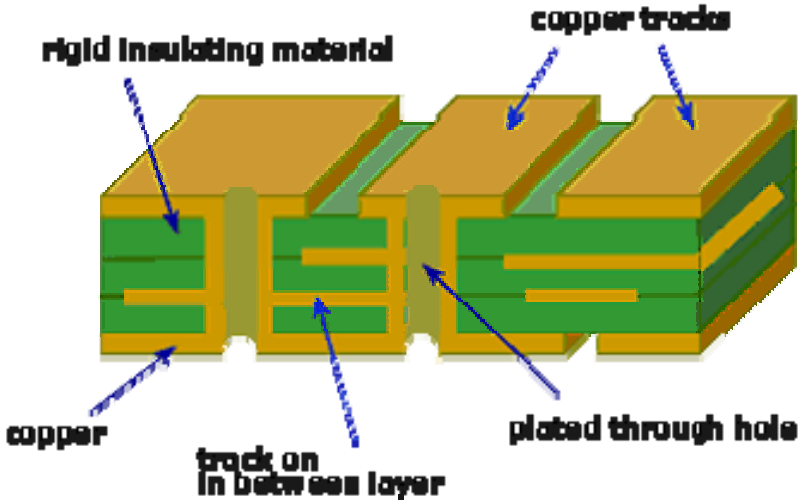
Leadframe



Now the board!



Single side



Two sided

Solder

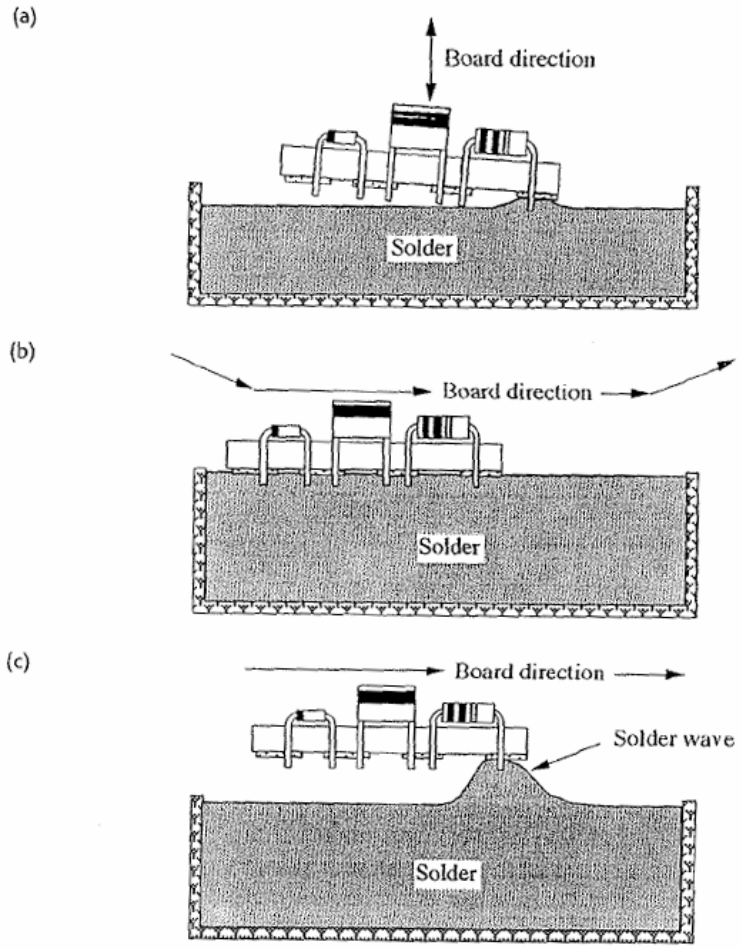
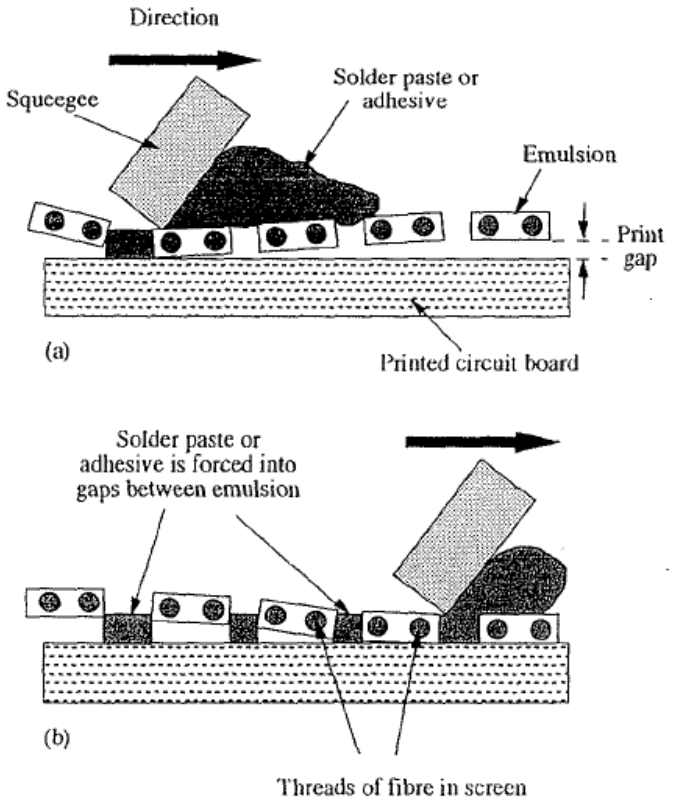
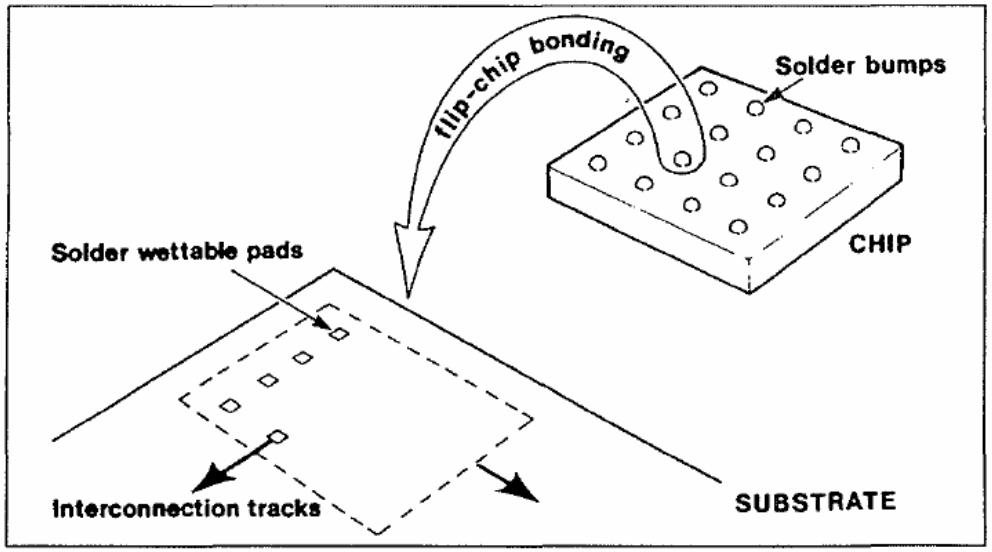


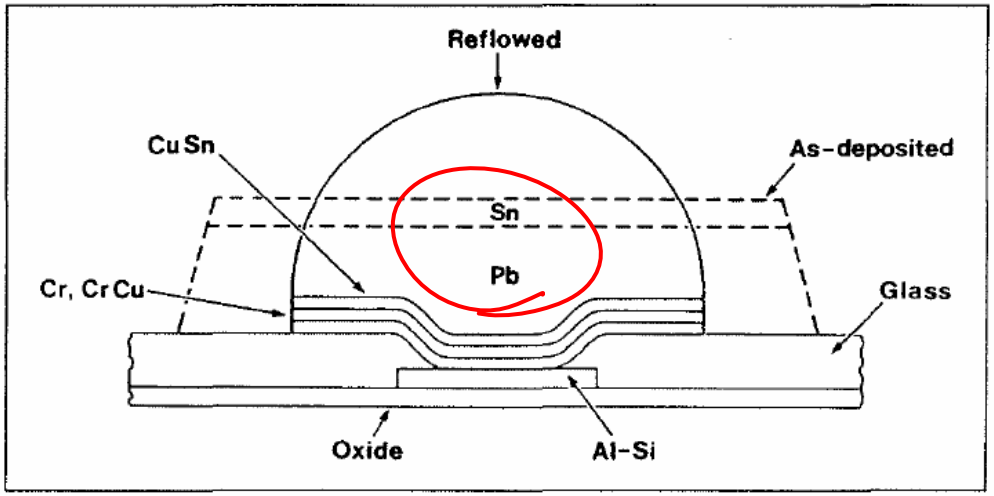
Fig. 4.16 CS soldering processes: (a) Dip (b) Drag (c) Wave (taken from *Soldering in electronics assembly* by Mike Judd and Keith Brindley, courtesy of Newnes).



ig. 4.17 Applying solder paste using the technique called 'silk screening' (not really silk any ıore!) (taken from *Soldering in electronics assembly* by Mike Judd and Keith Brindley, courtesy of ewnes).

Flip Chip





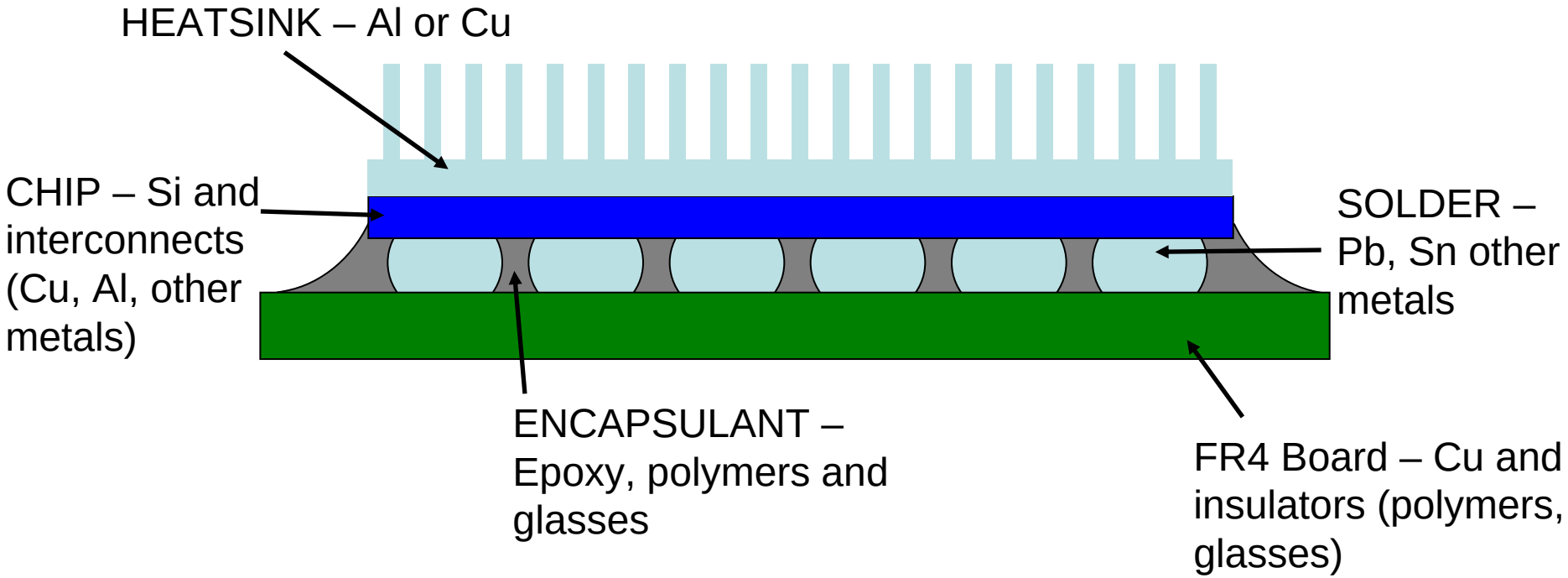
- Remember Day01?

Pb-free solder

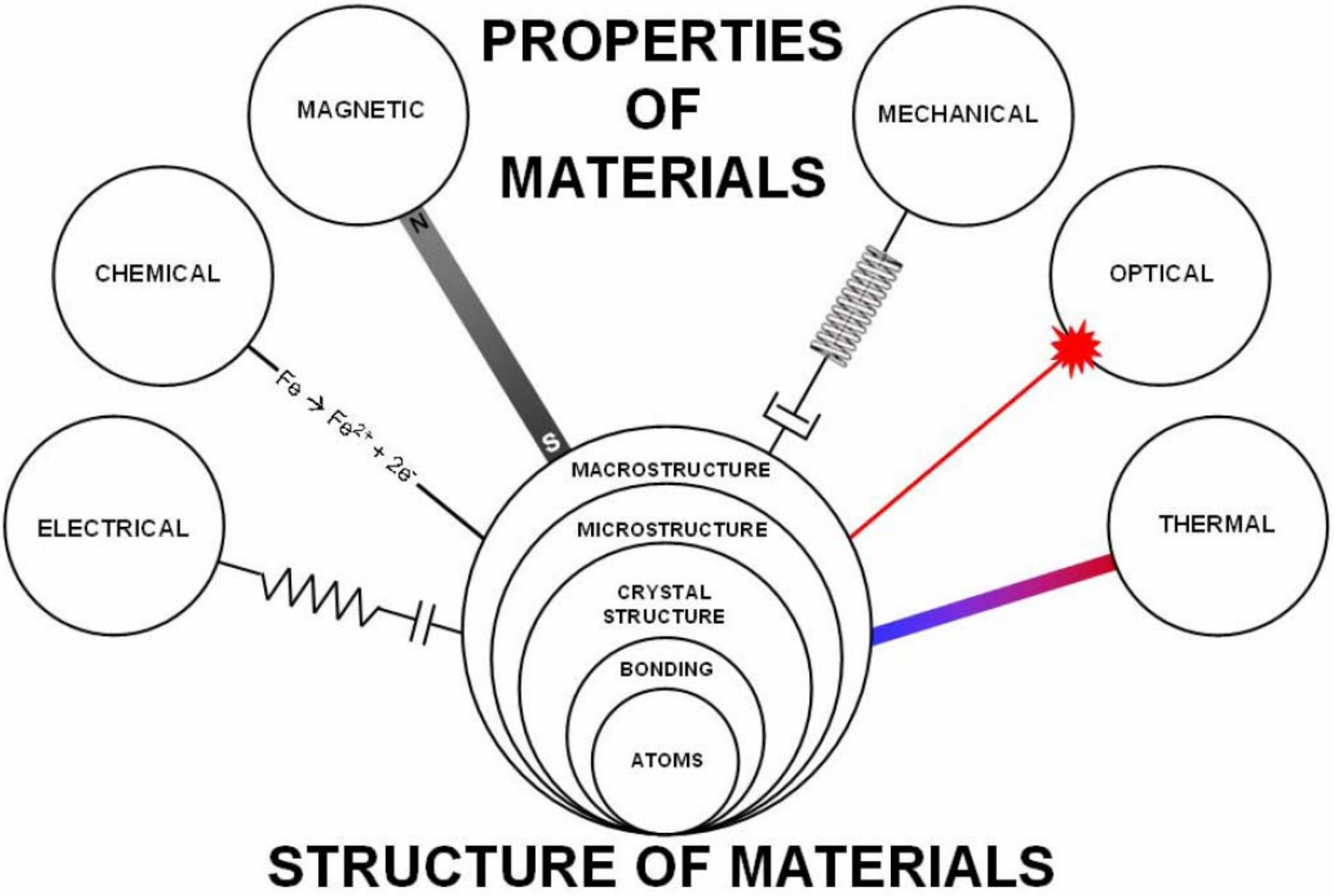
Pb-Sn

Sn-Ag-Cu

FLIP CHIP
BALL GRID ARRAY



FLIP CHIP
BALL GRID ARRAY


PROPERTIES
OF
MATERIALS
MAGNETIC
MECHANICAL
CHEMICAL
OPTICAL
N
S
Fe → Fe2+ + 2e-
ELECTRICAL
THERMAL
MACROSTRUCTURE
MICROSTRUCTURE
CRYSTAL
STRUCTURE
BONDING
ATOMS
STRUCTURE OF MATERIALS