ECSE 487 Computer Architecture Laboratory Term Project
Winter 2009
Description and Guidelines

Deliverables

- **abstract** (5%)
- **mid point reports and demonstration** (10%)
- **oral presentation** (20%)
- **report** (30%)
    - six page paper, IEEE professional paper style

Time Line

- Abstract: due February 16, 9:00 AM
- Abstract presentation: February 16 in class
- Midpoint 1 report: due March 2, 9:00 AM
- Midpoint 1 demonstration: week of March 2-6 in the lab
- Midpoint 2 report: due March 16, 9:00 AM
- Midpoint 2 demonstration: week of March 16-20 in the lab
- Miniconference: April 6, April 7, April 8
- Final report: due April 14, 9:00 AM

Please watch WebCT closely for updates, schedules and locations !!!!!

Group Signup

If your group composition has changed from Assignment 2 please email your group composition as soon as possible.

Project Topic

First and foremost: have fun! This project is your opportunity to explore the digital implementation of some topic which you find interesting. You might want to choose a topic that interested you from another course, or a personal interest.

For your term project you are to choose an interesting digital system, perform some preliminary "research" or a literature survey, design the system in VHDL, synthesize it for FPGA and gather statistics. You are free to choose any target FPGA you like (the most popular are by Xilinx and Altera and each company provides a wide range of FPGAs of different sizes, performance, extra features, etc).

The following lists some examples.

1. **Error detecting-correcting modules.** Some of the more advanced error correcting codes (other than Hamming codes) would be very interesting topics.
2. **Various communication network protocols** including ATM, SONET, Ethernet, FDDI, DBDQ, IBM token ring, high speed serial links or any recent development.
3. **Digital neural networks and fuzzy logic systems** to recognize patterns or perform processing.
4. **Multimedia digital systems** including MPEG, JPEG, speech/image or video compression and decompression systems, etc. Voice sub-band coding is one example; it can compress a 64 Kbit/s voice stream to about 8Kbit/s.
5. **Embedded special purpose processors** as applied to portable computing, rehabilitation, biomedical devices, etc.
6. **RISC CPU, DSP and computer subsystems**, for example, cache controller, schedulers, PCI bus interface.
7. **Hardware encryption/decryption units.** The AES, RSA, PGP, and DES algorithms are currently among the most popular.
8. **Fast designs for performing computer arithmetic algorithms**, i.e., multiplication, division, square roots etc., including transform function such as FFT, DCT, and Hadamard Transform.
9. **Image processing:** convolution masks, restoration, enhancement, coding, and so-on.
10. **Computational graphics:** hardware to perform image manipulations, i.e. moving the view to the left or right, zooming in or out, rendering, hidden line removal, etc. The field of computer graphics is full of interesting things to do with hardware including parts of a graphic pipeline and rendering algorithms.
11. FPGAs have been proposed for use in DNA pattern matchers, where they apparently outperform supercomputers. FPGA's hold appeal for the solution of many problems of a combinatorial nature.
12. Any interesting system you can think of. Search the FPGA manufacturer's "Application Notes" to get good ideas, and discussions of how to implement the systems on FPGA. You can implement a system or sub-system that is described in an Altera or Xilinx Application Note. Proceedings of conferences describe some of the research projects undertaken at other universities. There are international conferences and journals on the subject, which can give you ideas.

Here is a link to FPGA-related conferences:

http://www.ece.ubc.ca/~stevew/conf.html

A good journal is the IEEE Transactions on VLSI. However, there are many other journals in various application areas which also cover VLSI and FPGA implementations. All IEEE (and IEE) journals and conference proceedings are available at IEEE Xplore :

http://ieeexplore.ieee.org/

It is advised to construct smaller sub-systems of a larger system. For example, MPEG and JPEG compression systems often use 8x8 Discrete Cosine Transforms. You could just implement the DCT, which is a sub-system of the MPEG/JPEG systems. An important part of the paper would be a discussion about scalability. It is much more satisfying technically and intellectually to have a small design that works and is tested; and be able to predict the performance and requirements of a full scale version, rather than coming up with an unfinished and untestable large system.

Your project should use between 5,000 to 200,000 logic gates.

Software

One of the goals of this project is to show how hardware implementations can provide performance improvements over software implementations of an algorithm. Therefore, implement a software version of your algorithm. Then, calculate what the speedup is gained by your hardware implementation. Software simulation is a good first step in a hardware design. It is very difficult to build a hardware implementation without exploring the algorithm first in software.

Abstract and Abstract Presentation

Submit a written abstract by February 16 following the abstract guidelines below. The instructor will prepare an electronic version of your abstract which you will use for presenting your abstract in class later that day (therefore it is vital that you submit on time to give the instructor the rest of the morning to prepare the file). We will begin at 2:35 PM sharp! Please do not walk in late as a courtesy to your classmates who present in the early part of the class. Since we only have an hour, keep your presentation to about 5 minutes. We will provide you with feedback and suggestions. It would be a good idea to talk to us before to make sure your topic is reasonable or for help in finding a suitable topic.

Abstract Guidelines

Each group must submit a preliminary abstract of no more than 1 page to the course instructor by email at warren.gross@mcgill.ca, describing an outline of the chosen topic. Note that you do have flexibility and can deviate from your original plan while developing the project. However, in case of substantial deviation you will need to submit a new abstract so that the instructor is kept informed of your work. Also, a well written abstract is time saved since it can be reused in the final paper.

Please feel free to talk to us about possible topics anytime before the abstract due date.
The abstract will make up 5% of the course marks. The text should be submitted via email to warren.gross@mcgill.ca as a **plaintext file** with possibly one or two figures in PDF (preferred), TIFF or JPEG format.

The required **format** for your abstract is described below.

Format

```
Team:    Names of group members.

Title:   Meaningful and concise project title.

Abstract: Clear and concise overview and specifications of your
topic in 150-200 words.

References: List a few significant sources of information from
your research   (books, magazines, papers, conference
proceedings, application notes etc.) Follow the standard format
for quoting references used in IEEE papers or textbooks. For
information obtained from the Internet, it is insufficient to
simply write the link address.  You must state the document
titles and their authors pointed to by the links.
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The abstract should be submitted as **plain ASCII text** (i.e. not as a word processor file). In many cases, the abstract will make a much stronger case if it is supported by one or two diagrams and/or the key mathematical equations that describe the computational task that your device will perform. In such case, attach to your email such additional information as a PDF document (Adobe's portable document format, this is the preferred format) or TIFF, or JPEG picture format.

We have posted examples of many abstracts in an accompanying file. We urge you to begin your literature search as soon as possible. If you are unsure about a topic, please consult us.

Midpoint Reports and Reviews

Submit the first written midpoint report following the guidelines below by March 2 and the second by March 16. During the corresponding weeks we will arrange for you to demonstrate your progress to the TA in the lab.

Midpoint Report Guidelines

Each group must submit a two page document describing a preliminary design for their project (midpoint report 1). This includes "back of the envelope" calculations to estimate how many gates your design will require. There should be a section to discuss expected hardware complexity, i.e. how many gates are required, how fast the circuit might clock, etc. Again, a well written preliminary report is time saved since it can be reused in the final paper.

The second midpoint report (midpoint report 2) should describe your progress towards your goals, problems encountered and suggested approaches to tackle them. Each group will present their progress to the TA during individual 10 minute sessions. During that time, the group will have to convince the TA(s) that their design approach is valid and that they will succeed in completing the project. It's also a very good opportunity to get feedback. This exercise should also include a demonstration of prototype code or of working key subcomponents of the final project.

The text should be submitted via WebCT as a **plaintext file** with possibly one or two figures in PDF (preferred), TIFF or JPEG format.

The required **format** for your mid point reports is described below.

Format

```
Team: Names of group members.

Title: Meaningful and concise project title.

Abstract: Clear and concise overview and specifications of your
topic in 150-200 words (could be an updated version of the
initial abstract).

Progress review:
1. Estimates of final project achievement as above.
2. Discussion of design and results achieved so far.
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The report of one or two pages should be submitted as **plain ASCII text** (i.e. not as a word processor file).The report will be supported by one or two diagrams and/or key mathematical equations that describe the computational task that your device will perform. In such case, attach to your email such additional information as a PDF document (Adobe's portable document format, the preferred format) or TIFF, or JPEG picture format.

Oral Presentation

We will have a miniconference, much like a professional conference run by the IEEE or other professional societies. This is not only for grading, but it is for you to share your results with your classmates. Delivering a good technical presentation is a very important skill for engineers, no matter what their job function.

Some excellent guidelines for giving a talk are given in the posted guide by Prof. Kschischang.

We will provide you with a laptop and data projector. Please upload your files to WebCT as a .pdf file with the filename groupnum.pdf. You may use powerpoint to prepare the file but we recommend generating a .pdf file for the presentation. This is because fonts (especially math symbols) have a nasty habit of changing from computer to computer. A .pdf file will look the same on my computer as yours. Also, this avoids using the tempting animation features of powerpoint, which almost always detract from the message of your slides.

A 15 minute end-of-term oral presentation to the instructor and TA(s) illustrating what you have achieved.

- **Content**
  This area covers both design methodology and design implementation. As you have only 15 minutes, you will have to be selective on what you want to convey. The content of the talk must be consistent with what you have presented/are presenting in your paper. Key points should include the motivation for your project, an overview of your design approach, the challenges encountered and how you dealt with them. The results obtained from your study should be provided in some easily viewable graphical form and summarized briefly.

- **Organization**
  The content of the talk should be divided between the group partners and each should make clear the extent of his or her contribution to the project. There should be an introduction and conclusion to each component of the talk, albeit brief, and each component should link logically to the next.

- **Clarity**
  The talks should be rehearsed to make them smooth and comprehensible. The slides should be clear and understandable. The use of graphical data that is explained orally is generally a good approach. Reciting what is written on a slide usually results in a catastrophic presentation. The key is to use what is seen to show what cannot be said and say what cannot be graphically presented. Example: a mathematical equation, is hard to recite but is easy to show and to explain the meanings of the symbols, terms and factors and how they relate. Other examples, block diagrams, state transition diagrams, or waveforms: try to describe them without showing them!

- **Question Fielding**
  As some time will be earmarked for questions from the instructor, TA(s), and your fellow students, pointed and clear answers will contribute to the overall evaluation.

Written Report (30%)

A self-contained professional "paper" describing your project, its motivation, challenges, discussion of approach to problem solving, results and recommendations for future readers. **The paper must adhere to standard IEEE publication guidelines** (see Section "Publication Guidelines Below"). Please save your papers so that you can hand them in to your prospective employers!

A typical outline has

- an introduction and statement of purpose understandable by a non-specialist; and avoiding detail on background irrelevant to the project
- a high-level description of their design strategy
- description of challenges and method to address them
- description of the solutions
- qualitative and quantitative results
- Conclusion and recommendations
- Reference list.

Supporting Documentation

- A hardcopy of the most important reference (or two) should also be provided. If you used an Application Note, Conference paper or Journal paper as your main reference, provide a clean copy in your report.
- We suggest that you choose a topic which will allow you to design it, implement it on the FPGAs and then prepare a paper and presentation on what you have done. You are welcome to build upon what the previous projects in 487 or 494 have done, but as in any publication you must look up and reference any related prior materials and you must clearly explain you contributions.
- A listing of the professionally documented VHDL source code, adhering to the 2 column of UNIX "ink" type printout format, but with as many pages as necessary. This should also include any lengthy data such as tables and waveform that would use precious space in the main text. The main text would then say something like "Figure XX shows one representative example of test waveform (See Supporting Data for the full test set)".
- The paper, main reference and VHDL source code could be spiral bound in a booklet. In any case, an extra loose leaf copy of the paper must be provided so that it can be added into the next project compendium. Please keep a copy for yourself we will **not** return your project report.

Additional Suggestions

- See "Application Notes" provided by manufacturers such as Altera, Xilinx, Actel, QuickLogic, for ideas. Application notes usually target exciting, innovative and relevant designs, as we have listed above, and are usually provided on their web sites. The notes also describe how the designs can be implemented in FPGAs. Hence, these provide an excellent start - they usually have excellent topics, and they provide descriptions of how to implement the designs on FPGAs.
- See any recent conference proceedings on Programmable Logic Devices, Field Programmable Gate Arrays, Application Specific Integrated Circuits (ASICs), etc. These proceedings are full of papers describing what engineers in academia and industry are developing. Take note of how they organize and present their work.
- For a paper to be successful it must convey technical information in a concise and well organized manner. Useful information includes: how many gates does the design require according to analysis, how many gates does it require when

synthesized, how did you partition the design to implement it on a FPGA, how did you compile it, how fast can you clock it, what suggestions do you have for others, etc.

- We have been receiving many requests from local industry for EE. graduates skilled in VHDL, computer architecture and digital switching. If you write a good paper for the 487 Laboratory, you might want to show it to prospective employers.
- Don't pick a very difficult project topic. Try to select a topic which will allow you to build the system and simulate it in VHDL. If you are not sure about the topics, please come and see us.

Publication Guidelines

Below are listed the basic format guidelines for the paper, in the standard IEEE format.

- 6 to 8 pages in length
- 2 columns per page
- body text is 10 point font, single spaced
- Title (24 point font, centered in page)
- Authors and affiliation (11 point, centered)
- Abstract (9 point, 150 to 200 words, heading in italics, body in bold)
- Index terms (9 point, heading in italics, body in bold)
- Introduction, Design Methodology, Results, Analyses, Conclusions, and References (headings are 8 point, centered, upper case, numbered by roman numerals for main sections; 10 point, left justified, mixed case, numbered by upper case letters for subsections)
- All references should be located at the end of the paper but must be properly indicated in the body text. See any IEEE publications for the reference format.
- Justified text, font can be either Times or Times New Roman
- Margins: 1" from the edge
- Equations should be centered in columns
- Pages should be numbered

Sample paper style sheets are available from
http://www.ieee.org/web/publications/authors/transjnl/index.html