Computer Architecture Laboratory
ECSE 487B Winter 2009

Credits: 2 Credits (0-3-3) (Lectures, Labs and tutorials, outside work).
Instructor: Prof. Warren Gross
Office: McConnell 505
Phone: (514) 398-2812
Email: Warren.Gross@mcgill.ca
Office Hours: Contact to arrange a time.
TA: Laurier Boulianne (contact on myCourses)
Webpage: You are expected to check myCourses on a frequent basis for any Email, announcements, handouts, links and pointers, schedule changes, etc…There is a discussion board for course-related discussion.

Pre/co-requisites:
- Prerequisite: 455-206: Communication in Engineering.
- Co-requisite: 304-425: Computer Organization and Architecture.
- Experience with VHDL.

Calendar description: Basic software tools used in the design, synthesis and analysis of computer and communication systems such as data-paths, switching circuits, and arithmetic and logic circuits. Behavioral and structural modeling of hardware designs in the IEEE standard hardware description language VHDL. Synthesis and implementation of hardware designs using Programmable Logic Devices.

Lab: Computer Architecture Laboratory, ENGTR 4120. Hours: 24/7
Students should make use of the computer workstations in the Computer Architecture Laboratory (ENGTR 4120) as these have installations of the course software. Student versions of the course software can also be downloaded from the web for use on your home computer or laptop. Complete compliance with the McGill University codes of conduct concerning computer usage is expected and required.

TA tutorial and lab hours: TBD.

Class meetings: Monday 2:30 – 3:30 PM, ENGTR 0070. There will NOT be a meeting every Monday. The class schedule is listed below, but check WebCT often for any schedule changes. Attendance at all meetings is mandatory for all students.

Tentative Schedule (subject to change):

Lectures:

- January 5 : Introduction and logistics.
- January 12: Assignment 1 discussion. Due Jan. 26.
- January 19: Assignment 1 discussion continued if necessary.
- January 26. Assignment 2 discussion. Due Feb. 9.
- Feb 9: Project discussion.
- Mini Conference, April 6, April 7, April 8.

Schedule of Project Deliverables:

- February 16: Project abstract due.
- March 2: Mid point report 1 due.
- Week of March 2-6. Midpoint review 1 interviews.
- March 16: Mid point report 2 due.
- Week of March 16 – March 20. Midpoint review 2 interviews.
- Mini Conference, April 6, April 7, April 8.
- Project report due April 14.

Late submission policy for all due dates: No late submissions will be accepted. Medical notes will only be accepted within one week of the missed date.

Academic Integrity: All students are expected to be familiar with McGill's policies with respect to academic integrity: McGill University values academic integrity. Therefore all students must understand the meaning and consequences of cheating, plagiarism and other academic offences under the Code of Student Conduct and Disciplinary Procedures Procedures (see http://www.mcgill.ca/integrity for more information).

Course Texts:

P. J. Ashenden, The Designer's Guide to VHDL, Morgan Kauffman, 2nd edition.

Evaluation:
The overall course grade will be based on two assignments, and a final project. The project will involve writing and presenting an abstract, written midpoint reports and oral demonstrations, a final report, and a final presentation.

Grading Scheme: Assignment 1: **10%**, Assignment 2: **25%**, Project: **65%**.