Review of Basic Computer Architecture

ECSE 425

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Instruction Set Architecture (ISA)

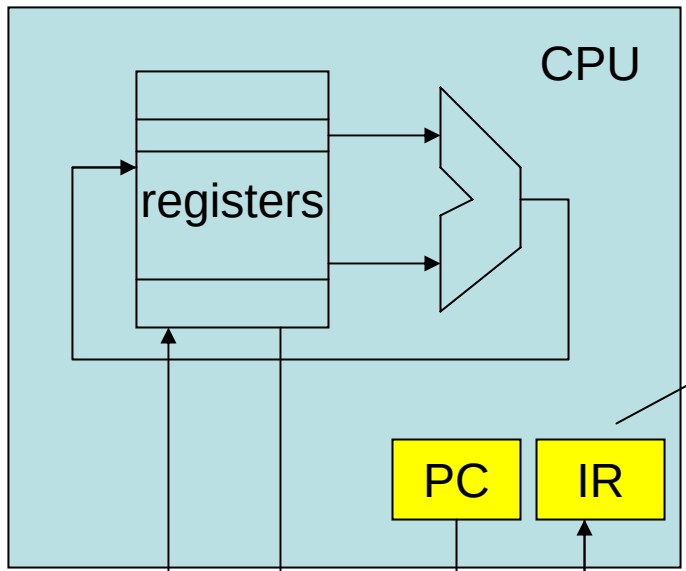
- Computers run programs made of simple operations called “instructions”
- The list of instructions offered by the machine is the “instruction set”
- The instruction set is what is visible to the programmer (really the compiler, although humans can directly program in “assembly language”).

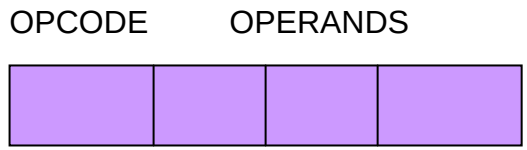
Instructions

- Two kinds of information in a computer:
  - instructions
  - data
- Instructions are stored as numbers, just like data
- Instructions and data are stored in the memory

Basic Computer Organization

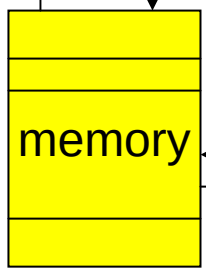
Limited number of **fast** registers for temporary storage





load

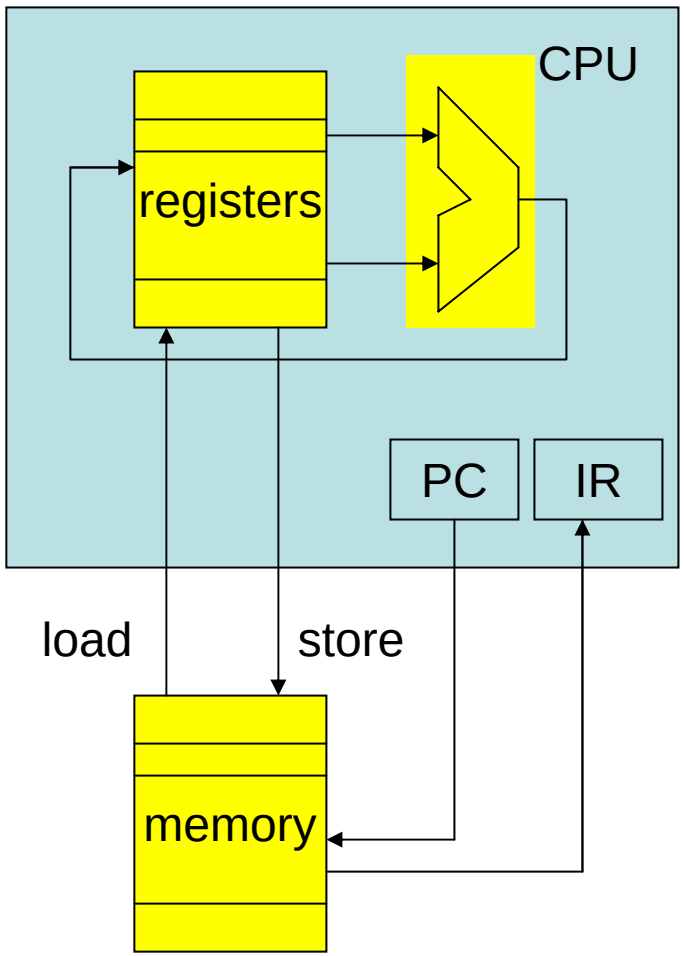
store



Large amount of **slow** memory Arranged as an array of bytes

Instructions are loaded into an Instruction register (IR) from the address pointed to by the program counter (PC). The PC is incremented by the instruction size (in bytes) for each new instruction. E.g. PC ← PC + 4

Load/Store Architecture (Reg-Reg)

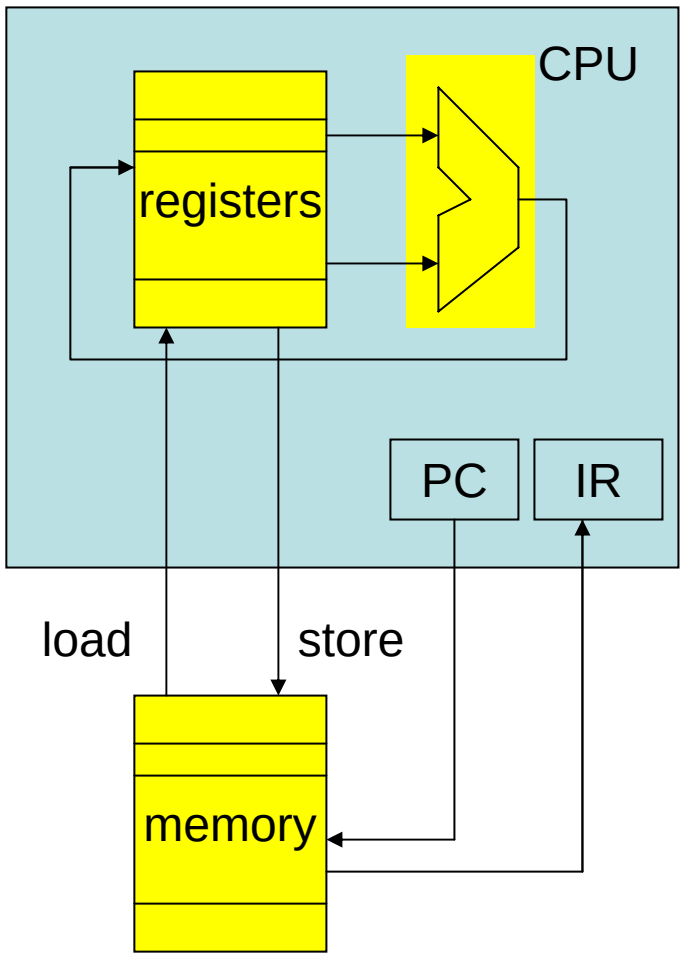


- Instructions can **ONLY** get their data and store their data from/to registers.

- The register numbers are specified in the operand fields of the instruction

- Since data is stored in memory, we need special “load” and “store” instructions for transfers between registers and memory. These two instructions are the ONLY ones allowed to access memory

Load/Store Architecture (Reg-Reg)



• **RISC** architectures are load/store. The regularity of this architecture enables fast organizations using pipelining (Appendix A).

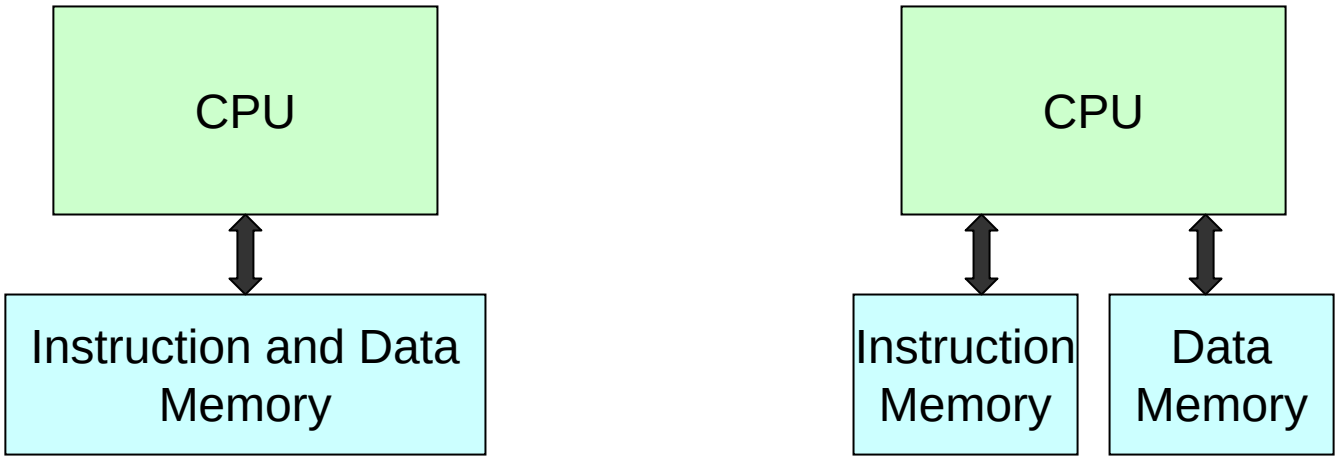
• **CISC** machines (e.g. Intel IA-32) permit instructions to get their data from both registers and memory (mem-reg). These highly irregular architectures (mem-reg, variable-length instructions) are practically impossible to pipeline.

• The advantage of them is that they produce shorter programs (no loads or stores needed, variable-length instr.d), but memory today is cheap and compilers can't really use complex instructions anyways.

• Modern "CISC" machines really just translate the CISC instructions to a set of RISC instructions and run those.

  • done purely for compatability reasons.

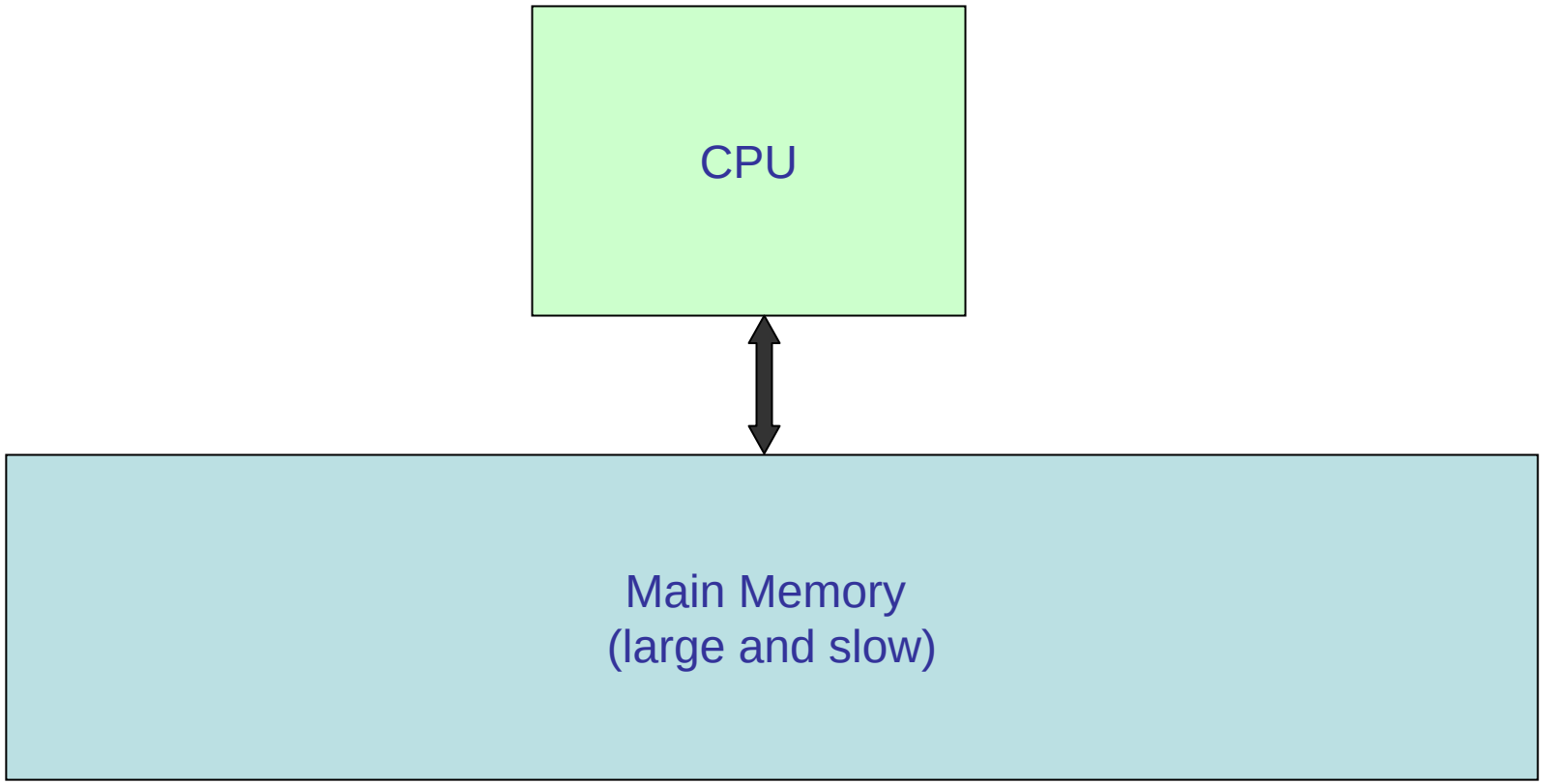
Harvard vs. Von Neumann Architectures



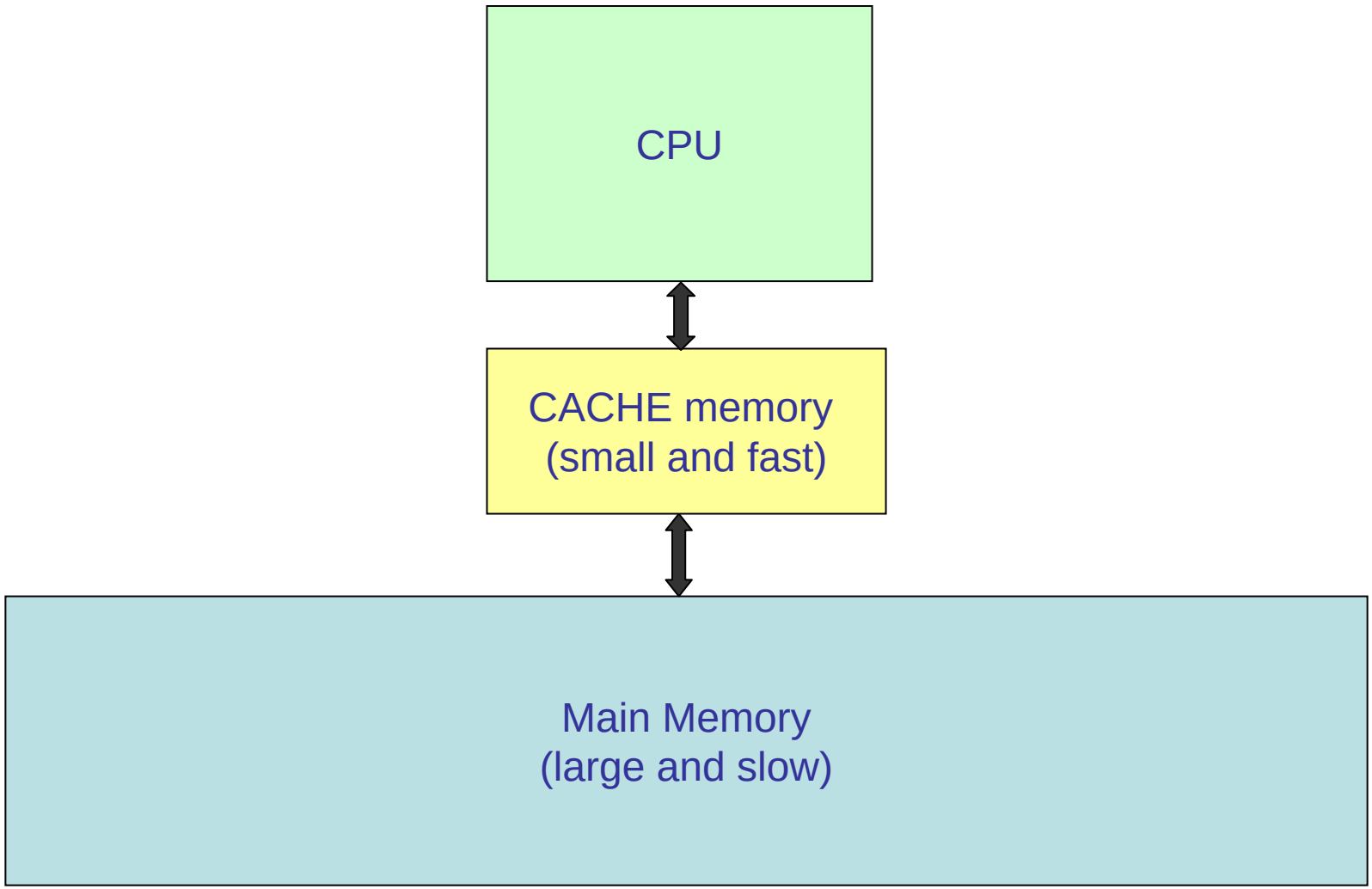
Von-Neumann

Harvard

Cache Memory

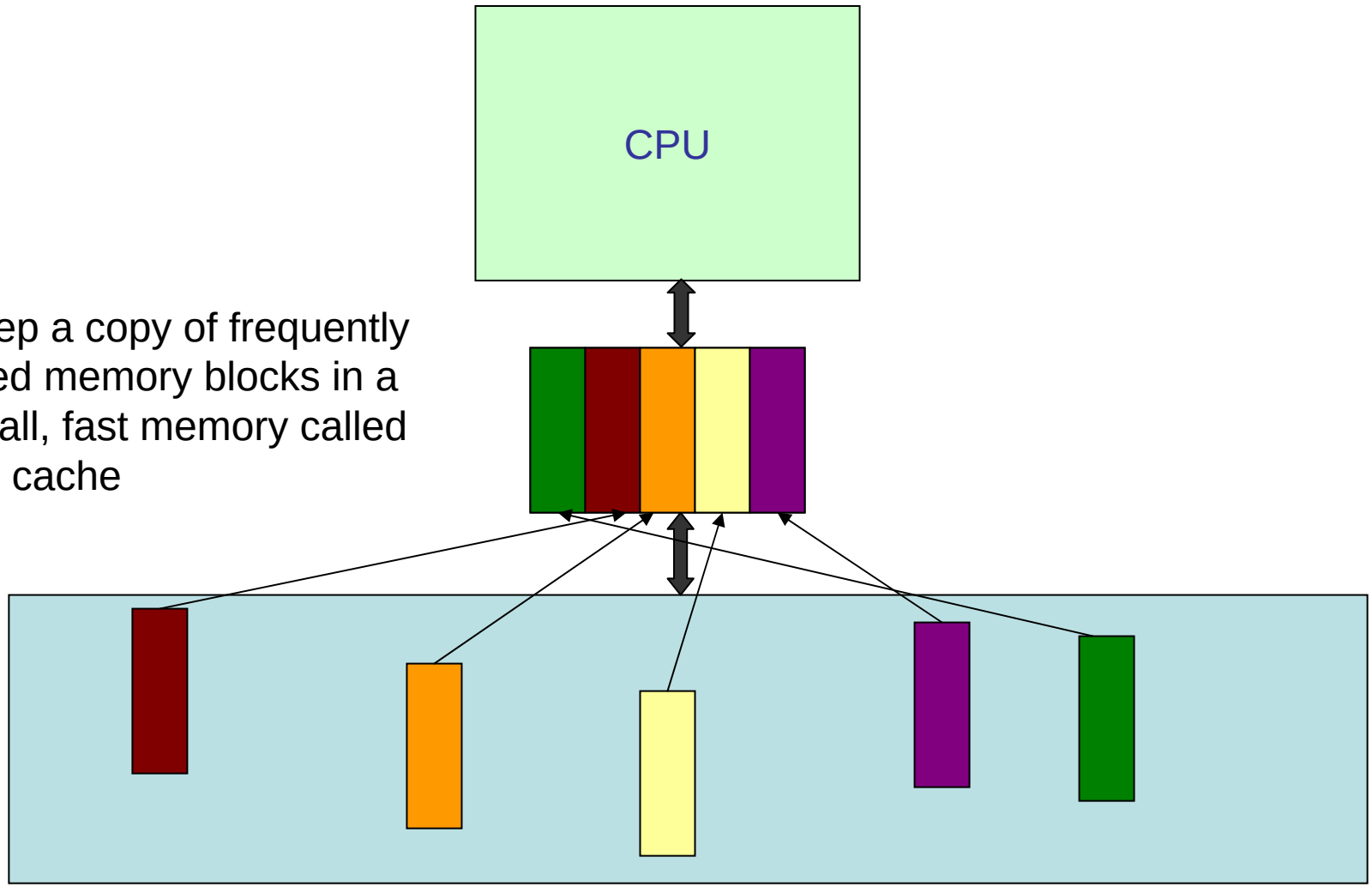


Cache Memory



Cache Memory

Keep a copy of frequently used memory blocks in a small, fast memory called the cache



Cache Architectures