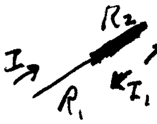
Real-Time Systems ECSE 431
Assignment 5: exam *answers*

1)Your embedded system is context switching continuously between *running* tasks without accomplishing anything useful. What is this an example of? What if they need each other's resource to get out of this quandary; what is that an example of?

[illegible] → (no resources involved)

a) livelock
b) spinlock (not deadlock because tasks are running)

2)You are building an external interrupt circuit board. The difference in impedances between two lines that connect is causing some backward echo current. Describe this backward current in terms of the initial current I coming down the line and the two impedances R_1 and R_2.



$I = I_2 - I_1$

echo current $= I_1$

$I_1 = I_2 - I$

$I_1 = \frac{R_1}{R_2}(I - I_1) - I$

$IR_1 = I_1R_1 + I_2R_2$

$I_2 = \frac{R_1}{R_2}(I - I_1)$

extra credit: a double reflection is more dangerous because it doubles the ISR trigger rate loading down the system.

$I_1 = I\left(\frac{R_1}{R_2} - 1\right) / \left(\frac{R_1}{R_2} + 1\right)$

$I\,\dfrac{\left(\frac{R_1 - R_2}{R_2}\right)}{\left(\frac{R_1 + R_2}{R_2}\right)} = I\,\dfrac{R_1 - R_2}{R_1 + R_2}$

3)Write the Schrodinger's equation for an electron in a 1-dimensional potential well of size V in terms of its wave function and total energy. List 3 possible reasons an electron could escape this potential to enter a conduction band in a semiconductor for instance.

this is extra credit →

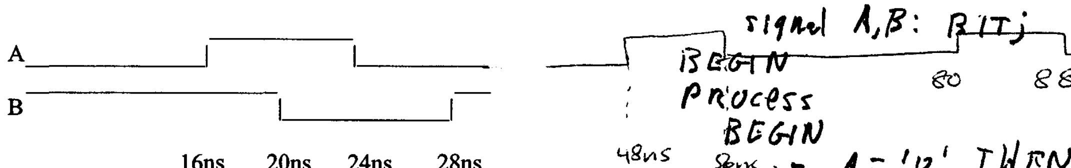
$$-\frac{d^2\Psi(x)}{dx^2} + V\Psi(x) = E\Psi(x)$$

1) light absorption
2) thermal energy
3) electric field

4)Why use MRAM over SRAM? Give 4 reasons.

1) space density factor 100 greater
2) less power needed (10^{-4}eV/B vs 10^{-11}eV/E needed)
3) faster to access (.5ns vs 2ns)
4) power consumption is less due to backward EMF $= IR + L\frac{dI}{dt}$ in standard SRAM trans

5)You have the following signals you wish to model in VHDL where B depends on A, which has a pulse with a 32 ns period.



Write an ARCHITECTURE routine to describe this **pulsed** behavior using transport delay modeling.

```
ARCHITECTURE signals IS
  signal A,B: BIT;
BEGIN
  PROCESS
  BEGIN
    IF A = '0' THEN
      A <= '1' AFTER 24NS;
    ELSE
      A <= '0' AFTER 8NS;
    ENDIF
    B <= TRANSPORT NOT A AFTER 4NS;
  END PROCESS;
```

48ns 56ns 80 88

Real-Time Systems ECSE 531
Assignment 5: exam answers

6)The data thruput that your uprocessor can handle has been measured to be 1 GByte/sec. The average data read/write request is 10 bytes in size. If the cache can be accessed in 10 nsec and the main memory accessed in 100 nsec, what is your cache hit rate?

$1\,GB/sec = 10B/[x \cdot 10\,nsec + (1-x)\cdot 100\,nsec]$

$\Rightarrow 100\,nsec - 90x\,nsec = \frac{10B}{1\,GB/sec} = 10\,nsec \Rightarrow x = 1 \Rightarrow 100\%\ hit\ rate$

7)In question 6, it has been determined that the jitter in your processor's performance is due to inexact number of bytes that are transferred per hit in the cache. Specifically, there is a 10 byte +/- 2 byte spread in your average data transfer. What is the jitter due to this spread?

$\frac{2\ bytes}{1\,GB/sec} = 2\,nsec$

8)In question 7, the total jitter in the real-time system is 4 nsec. What is the total jitter due to all contributions not counting the cache contribution?

$jitter = \sigma_T = \sqrt{\sum_i \sigma_i^2} = \sqrt{2^2 + \sum_{i+1} \sigma^2} = 4$

$\Rightarrow 16 - 4 = \sum_{i+1} \sigma^2 = 12 \quad \sqrt{\sum \sigma^2} = \sqrt{12}\ nsec$

9)What are the 3 general types of embedded systems, and what is the advantage of each?

distributed → cost effective, can be broken into parts.
mission critical → safe, can't fail, speed not an issue
signal processing → fast, safety not an issue

10)I have a critical section of memory that is utilized in parallel by 2 independent tasks. What do I use to protect this memory from a race condition?

a global semaphore or
independent semaphores that can communicate with each other