```
ENTITY serial_adder IS
     PORT( a,b, start, clock: IN BIT; ready: OUT BIT; result:
     BUFFER BIT_VECTOR (7 DOWNTO 0);
END serial_adder;

ARCHITECTURE behavior of serial_adder IS
     SIGNAL clock:  BIT;
BEGIN
     PROCESS(clock)
          VARIABLE count: INTEGER = 8;
          VARIABLE sum, carry: BIT;
     BEGIN
          IF (clock = '0' AND CLOCK'EVENT)THEN
               IF start = '1' THEN
                    count = 0;
                    carry = '0';
               ELSE
                    IF count < 8 THEN
                         count = count + 1;
                         sum = a XOR b XOR carry;
                         carry = (a AND b) OR (a AND carry) OR
                              (b AND carry);
                         result <= sum & result (7 DOWNTO 1);
                    END IF;
               END IF;
               IF count = 8 THEN
                    ready <= '1';
               ELSE
                    ready <= '0';
               END IF;
          END IF;
     END PROCESS;
END behavior;
```