ECSE 420, Fall 2005

Midterm Examination

1. (Performance bounds- 15 points) Plot Amdahl's and Gustafson-Barsis bounds as the functions of the serial part and the number of processors. Show the calculation for a number of characteristic cases of your choice. Show on the graph how the fixed overhead impacts both bounds.

2. (Bus communication requirements – 15 points) Consider a bus-based machine with 4 processors, each running at a 0.5 GIPS and running a workload that consists of: 50% ALU operations, 20% loads, 10% stores and 20% branches. Suppose that the cache miss rate at each processor is1% for instruction cache and 2% for data cache, and that the cache sharing among 2 processors is 40% and zero otherwise. The system bus bandwidth is 7.5GB/s. Assuming that the cache line is 32 bytes large, and a snooping protocol, determine the bandwidth used. How many processors could the bus accommodate?

3. (Snooping Cache Coherence – 15 points). Consider a 4-processor machine running the Illinois protocol that uses a wired-OR signal indicating the shared state. Show a sequence of bus events where three processors read a cache line, followed by two processors writing to it. Indicate the status of this cache line at each node throughout the process. Assume no cache-to-cache transfers and that the memory always supplies the cache line (as opposed to the processor cache).

4. (Communication cost – 15 points) For a machine with the communication overhead, assist occupancy and network delay (message start-up time) of 500 ns and the asymptotic peak bandwidth of 2 GB/s, calculate the message lengths for reaching the 1/3rd and 2/3rd of the peak bandwidth. Assuming that the contention at these two points adds 100 and 500 ns to the start-up time, respectively, what message lengths would then be obtained?

5. (Directory scheme – 10 points) For a directory machine model given in the class, describe the action taken upon a processor writing a cache line for which the dirty bit is set to ON. Describe what happens to the presence bits.

6. (Synchronization – 15 points) You have been just hired to add the multiprocessor support into a simple RISC processor designed by your employer (a processor of your choice, such as DLX). You decide that it is most critical to add LL and SC instructions. Describe what would you do at the architectural level. Separate the basic operation correctness from the performance optimizations that you would employ.

7. (Hierarchical design – 15 points) You are preparing to enter the market with a machine that uses the multi-core processors as building blocks. The 4-core processors use snooping as the basic cache coherence scheme, but your machine will be scalable and use the directory cache coherence. What design steps would you undertake to make such a scalable multiprocessor? Draw a simplified system diagram, and outline the cache coherence scheme. If the 95% of cache invalidations for the target applications concern 2 processors, describe how this fact would guide your design decisions.