ECSE 420-Parallel Computing
Assignment 3

1. A shared-bus SMP 4-processor system uses the write-through invalidate protocol for cache coherency. If each processor runs at 2.8 GHz with 2.2 CPI and has cache blocks of 16 bytes, find the percentage of instructions that must be stores to saturate a 2 GB/s bus.

2. For the following systems, state whether or not the caches provide inclusion naturally. If not, state the problem or give an example that violates inclusion:

a. L1: 8-KB direct-mapped primary instruction cache, 32-byte line size 8-KB direct-mapped primary data cache, write through, 32-byte line size
L2: 4-MB four-way set-associative unified secondary cache, 32-byte line size

b. L1: 16KB direct-mapped unified primary cache, write-through, 32-byte line size
L2: 4-MB four-way set-associative unified secondary cache 64-byte line size

3- Compared to a shared first-level cache, what are the advantages and disadvantages of having private first-level cache bust a shared second-level cache?

4. Assume that each processor has separate instruction and data caches and that there are no instruction misses. Further assume that, when active, the processor issues a data cache request every 3 clock cycles, the miss rate is 1%, and miss latency is 30 cycles. Assume that tag reads take 1 clock cycle but modifications to the tag take 2 clock cycles.

a. Quantify the performance lost to cache tag contention if a single-level data cache with only one set of cache tags is used. Assume that the bus transactions requiring snoop occur every5 clock cycles and that 10% of these invalidate a block in the cache. Further assume that snoops are given preference over processor accesses to tags. Build a simple simulator.

b. What is the performance lost to tag contention if separate sets of tags for processor and snooping are used?
c. In general, would you give priority in accessing tags to processor references or bus snoops?

5. Although the challenge supports the MESI protocol states, it does not support the cache-to-cache transfer feature of the original Illinois MESI protocol.
(a) Discuss the possible reasons for this choice.
(b) Extend the challenge implementation to support cache-to-cache transfer. Describe the extra signal needed on the bus, if any and keep in mind the issue of fairness.
(c) Although the challenge MESI protocol has four states the tags stored with the cache controller chip keep track of only three states (I, S, and E+M) Explain why this is still works correctly. Why they made this optimization?