Problem Set 7

❒ The Cascode Amplifier (Section 6.8):

- Problem 6.105 in the textbook
- Problem 6.107 (a and c only) in the textbook

❒ Differential Cascode Amplifiers (Sections 6.8 and 7.5) and Advanced Current Mirrors (Section 6.12)

• Problem1:

Figure 1 shows a differential *cascode* amplifier with an active load formed by a Wilson current mirror.

Figure 2 shows a differential *folded-cascode* amplifier with an active load formed by a modified Wilson current mirror. Both the cascode amplifier (in Figure 1) and the folded-cascode amplifier (in Figure 2) apply a differential common-base stage to the input differential pair. However, the folded-cascode amplifier uses cascode transistors opposite in type from those used in the input stage. **This arrangement of opposite-type transistors allows for the output of the amplifier to be taken at the same bias-voltage levels as the input signals.**

For the amplifiers in Figures 1 and 2:

Assume that the bias-voltage level at the output is stabilized by negative feedback (to about 0 V) and that all BJTs are in the active region. When finding the dc currents, ignore the base currents of every transistor.

A) What is the dc bias current in transistors Q_1 and Q_3 (in terms of I).

B) Find an expression for:

- the amplifier input resistance R_i
- the amplifier output resistance R_o

  Hint: the output resistance of the Wilson current mirror (Q_5-Q_7) is approximately $\beta r_o/2$.
- the short-circuit transconductance G_m (where $G_m \equiv i_{\text{out}} / v_{\text{in}}\big|_{R_L = 0}$)

  and draw the equivalent transconductance circuit model of the amplifier.
- the open-circuit small-signal voltage gain A_v (where $A_v \equiv \left.\dfrac{v_{\text{out}}}{v_{\text{in}}}\right|_{R_L = \infty}$)

C) Assume that, for proper operation, the minimum voltage drop across any of the current sources is V_{CS}.
Find an expression for:

- the smallest value $V_{\text{BIAS, min}}$ of V_{BIAS} in Fig. 1, with cascode transistors $Q5$-$Q7$ in the active mode.
- the largest value $V_{\text{BIAS, max}}$ of V_{BIAS} in Fig. 2, with cascode transistors $Q5$-$Q7$ in the active mode.
- the input common-mode voltage range and the output voltage range, over which the amplifier behaves as a linear amplifier for small-signal differential inputs (i.e., over which all BJTs are in active mode).
- simplify the above expressions, assuming:

$$|V_{CS}| = |V_{\text{CE, sat}} + V_{\text{BE, }on}| \quad \text{and} \quad |V_{CEsat}| = |V_{\text{BE, }on} - V_{\text{BC, }on}|$$

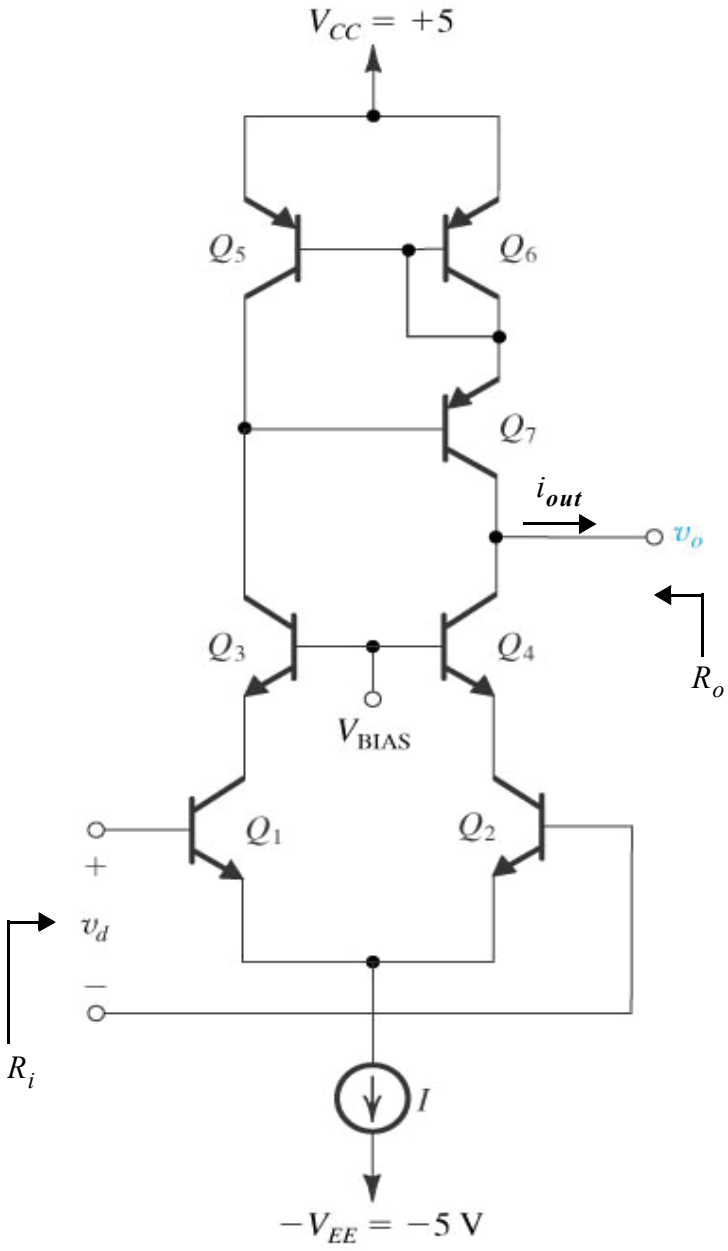


Figure 1 (Fig. P7.74)

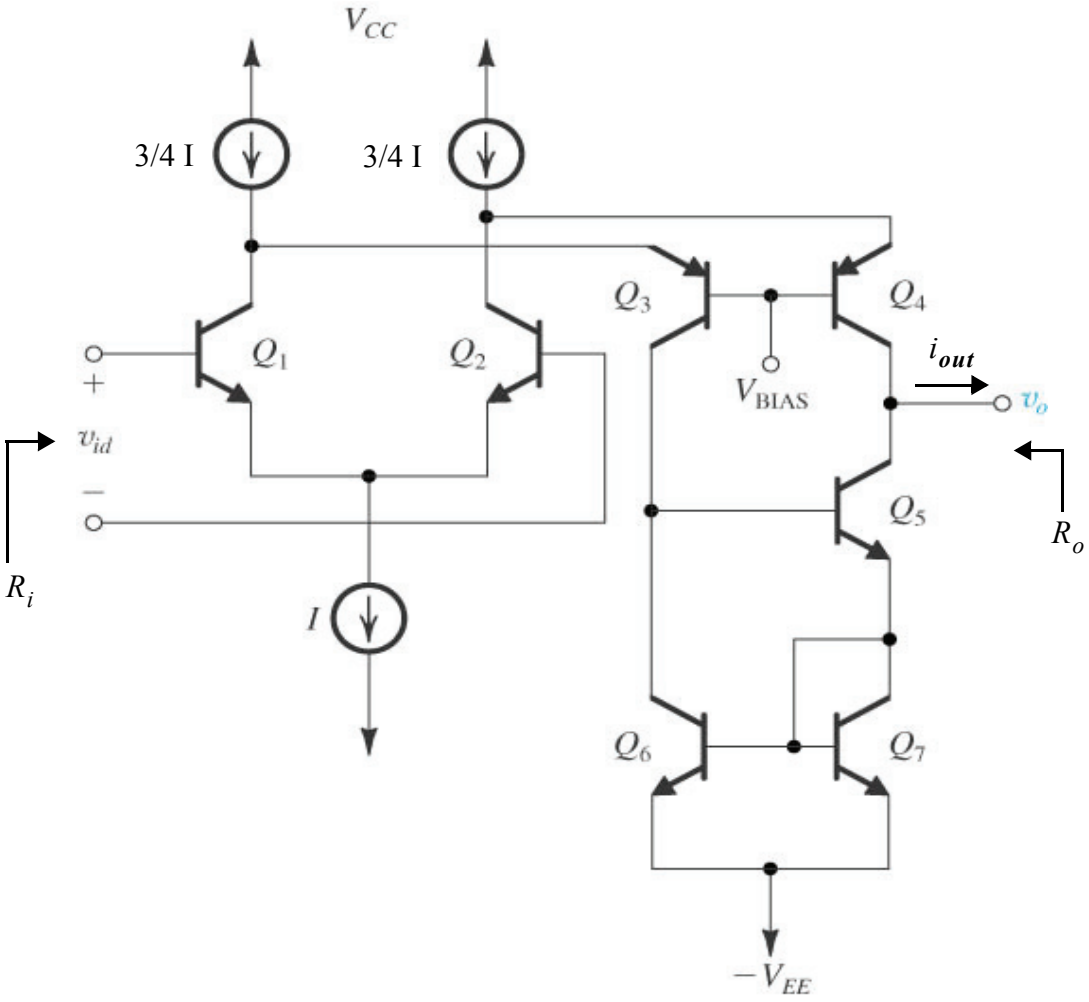


Figure 2 (Fig. 7.35)

- **Problem 2:**

D7.75 Consider the bias design of the Wilson-loaded cascode differential amplifier shown in Fig. P7.74.**(Figure 1)**

(a) What is the largest signal voltage possible at the output without Q_7 saturating? Assume that the CB junction conducts when the voltage across it exceeds 0.4 V.
(b) What should the dc bias voltage established at the output (by an arrangement not shown) be in order to allow for positive output signal swing of 1.5 V?
(c) What should the value of V_{BIAS} be in order to allow for a negative output signal swing of 1.5 V?
(d) What is the upper limit on the input common-mode voltage v_{CM}?

❒ High-Frequency Response of Cascode Amplifiers (Sections 6.6 and 6.8)

• Problem 3:

For the amplifiers in Figures 3 and 4, derive an expression for:

i) the midband voltage gain $A_M = v_o / v_s$;

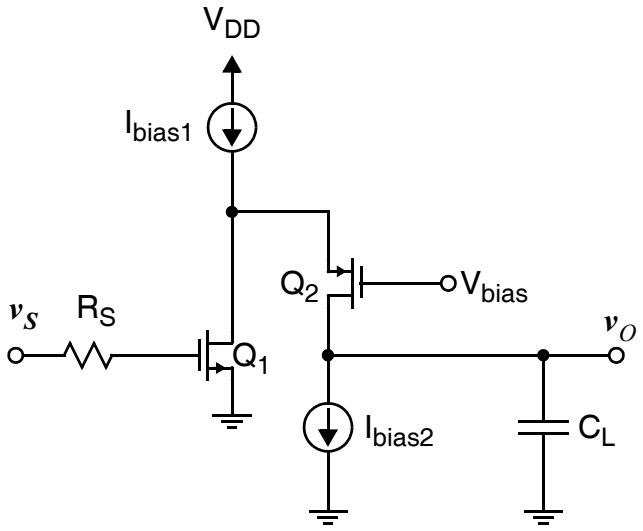
ii) the 3dB-frequency ω_H, assuming a dominant pole exist.

Hint: Follow the following steps to find ω_H:

1) apply Miller's theorem;
2) find the open-circuit time constants (poles) associated with each node;
3) find ω_H based on the open-circuit time-constant approximation, assuming a dominant pole exists.

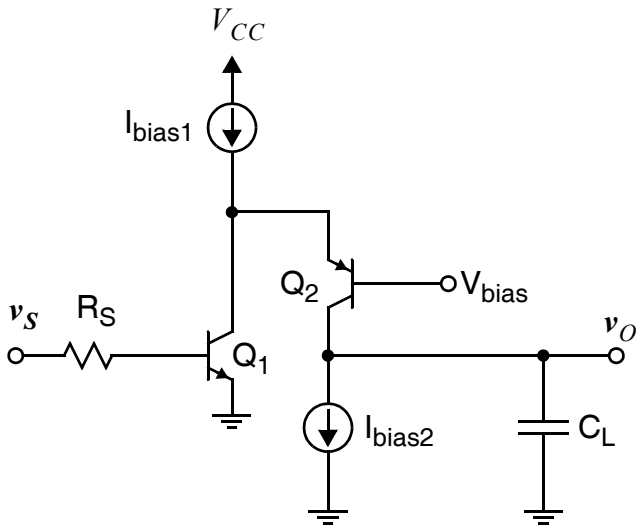
Assume:

- Biasing:
  - each current source has an output resistance of R_L.
  - the dc-bias voltage level at the output is stabilized by negative feedback, with all BJTs and MOSFETs biased in the active and saturation modes, respectively.
- For the MOS amplifiers in Figure 3.:
  - the body effect is negligible.
  - the substrate (Body) terminal of the NMOS transistors is connected to *GND*.
  - the substrate (Body) terminal of the PMOS transistors is connected to V_{DD}.
- For the BJT amplifiers in Figure 4:
  - neglect the small-signal base resistance r_x.



(a) MOS Folded-Cascode Amplifier

Figure 3. MOS amplifiers.



(d) BJT Folded-Cascode Amplifier

Figure 4 BJT amplifiers.