McGill

ECSE 304-334

Introduction To Microelectronic Circuits

Final Examination
Thursday Dec. 13, 2007
2:00 PM - 5:00 PM

Examiner: Prof. G. Roberts GR
Associate Examiner: Prof. V. Chodavarapu VPL

Name: _____

Student No.: _____

Instructions:

- Answer all 5 questions.
- Questions have equal weight; Distribution is indicated in brackets.
- Answer directly on the question sheet provided. You may use the back of the sheet to continue your answer.
- Only the sheets provided will be marked.
- This is a **Closed-Book Exam**; A **one-sided** handwritten **Crib Sheet** is allowed.
- Write your name and student number on the top of this sheet and on the top of each of the question sheets that you want marked.
- Only the faculty-approved **Standard Calculator** is permitted.
- You are permitted **Translation** dictonaries ONLY.

Note To Student:

The instructor and / or his representative cannot and will not answer any questions during the final examination period. If you believe a question is in error or requires further clarification, please state your assumptions and work the problem from this point onwards. Clearly, if a question is in error, you will recieve full benefit.

Marking Scheme:

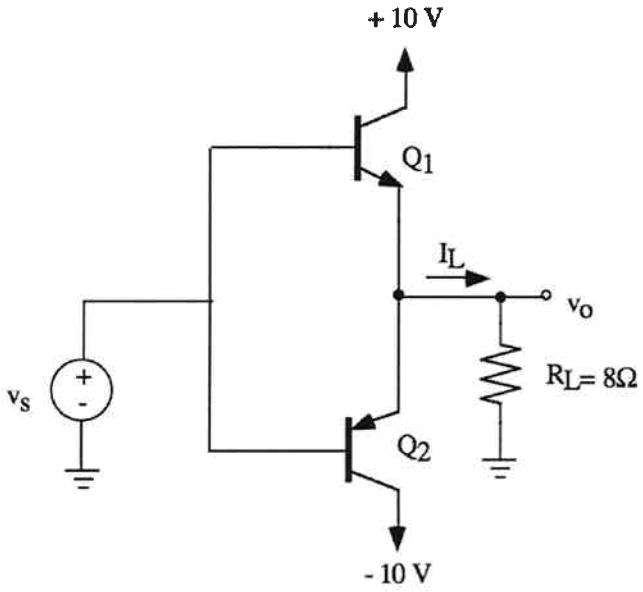
Q1 (10 points)	*Q2 (10 points)*	*Q3 (10 points)*	*Q4 (10 points)*	*Q5 (10 points)*	*TOTAL*

Question 1:

(a) Sketch the ideal input-output transfer characteristic for the above amplifier, i.e., v_o vs. v_s , and identify critical points and slopes.

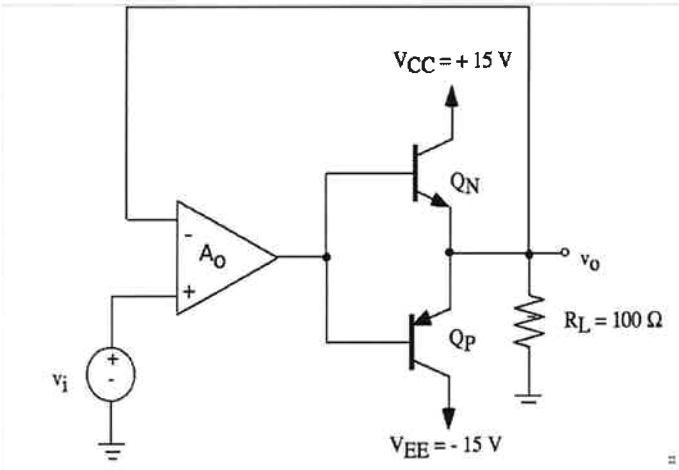
Sketch the output signal when a sinewave of 10 V peak amplitude and zero offset is applied as input.

Assume that the cut-in voltage for each transistor is 0.5 V and that $V_{CEsat} = 0.3$ V.



▶ **[2 points]**

(b) A modified class B BJT power amplifier of the type shown in the figure to the right is driven by a sinewave input of 10 V peak centered around 0 V.



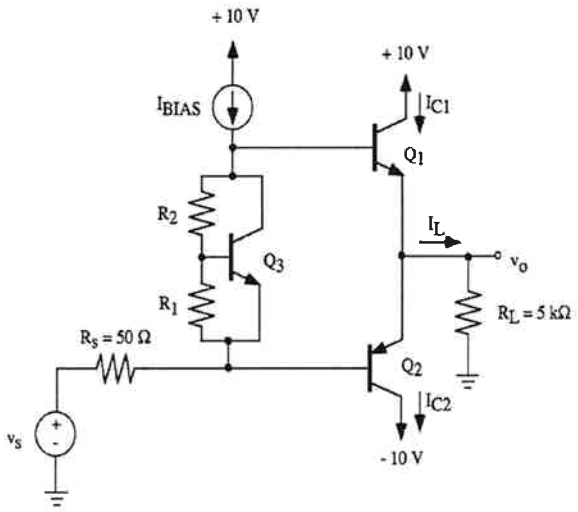
Find the time-average power dissipated in the load, the time-averaged power dissipated in the transistors, the power drawn from the power supplies and the amplifier efficiency.

► [5 points]

Question 1(b) ..... Continued .....

(c) Consider the following class AB output stage. I_{BIAS} is assumed to be an ideal current source. Select values for R_1, R_2 and I_{BIAS} such that the quiescent current I_Q for Q_1 and Q_2 is 0.1 mA and that the maximum output load current is 50 mA. All transistors are characterized by:

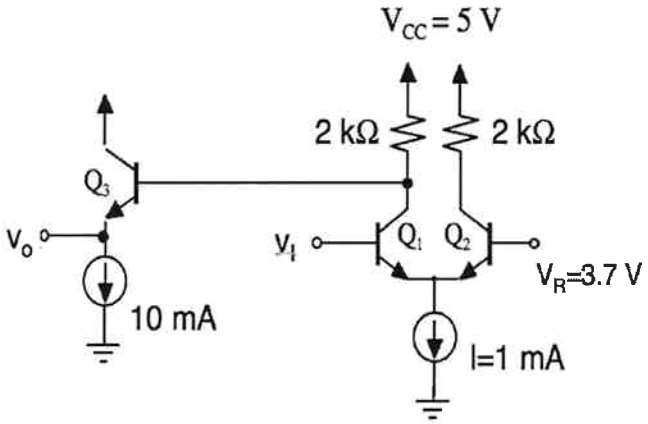
$I_s = 10^{-15}$ A, β=100, and $V_A = 50$ V.



► **[3 points]**

▼ *Question 2:*

The figure on the right shows a logic inverter based on a differential pair. Here Q_1 and Q_2 form a differential pair, whereas Q_3 is an emitter follower that performs two functions: It shifts the level of the output voltage to make V_{OH} and V_{OL} centered on the reference voltage V_R, thus enabling one gate to drive another, and provides the inverter with a low output resistance.



Assume all transistors have $V_{BE} = 0.7$ V at $I_C = 1$ mA and have $\beta=100$.

► **Answer the following questions.**

(a) For v_I sufficiently low so that Q_1 is cut-off, find the value of the output voltage v_O. This is V_{OH}.

► **[1 point]**

(b) For v_I sufficiently high so that Q_1 is carrying all the current I, find the value of the output voltage v_O. This is V_{OL}.

▶ [1 point]

(c) Determine the value of v_I that results in Q_1 conducting 1% of I. This can be taken as V_{IL}.

► [2 points]

(d) Determine the value of v_I that results in Q_1 conducting 99% of I. This can be taken as V_{IH}.

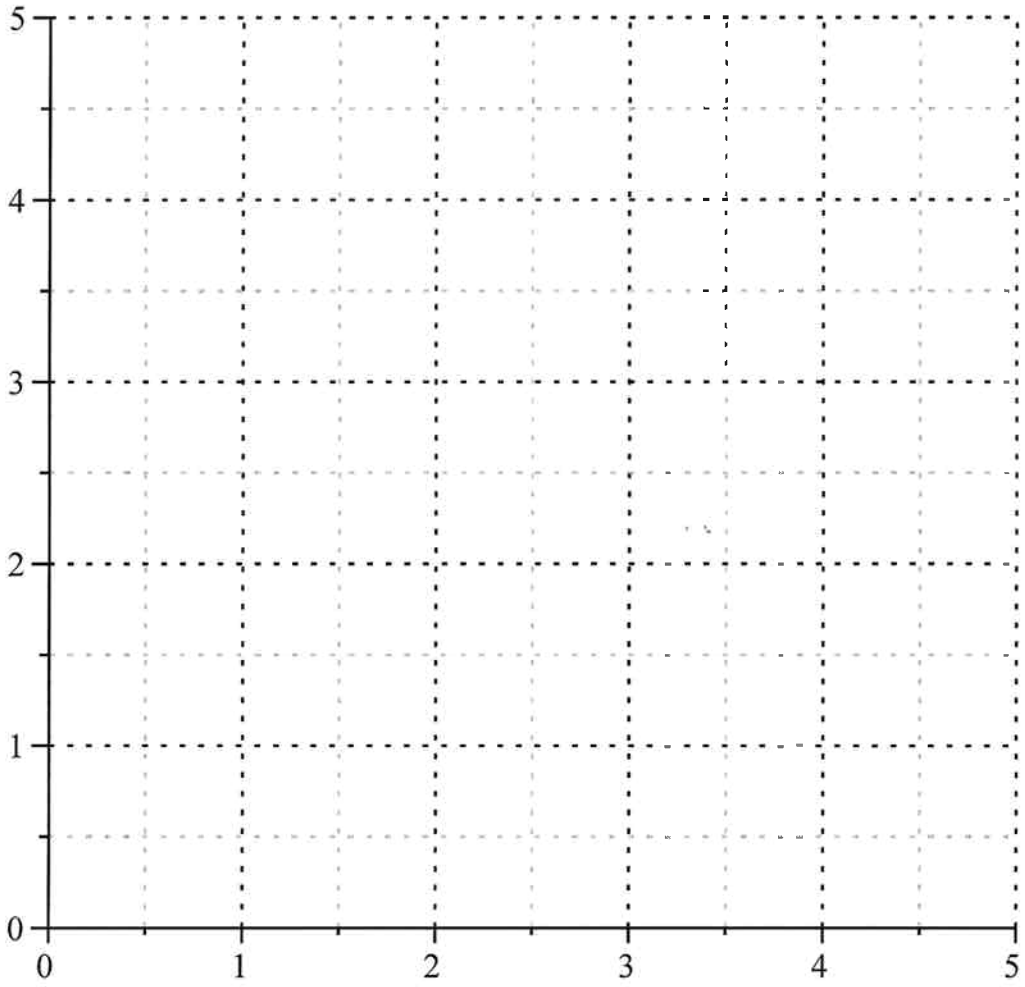
▶ **[2 points]**

(e) Calculate the noise margins which are defined as: $NM_H=V_{OH} - V_{IH}$ and $NM_L=V_{IL} - V_{OL}$.

▶ **[1 point]**

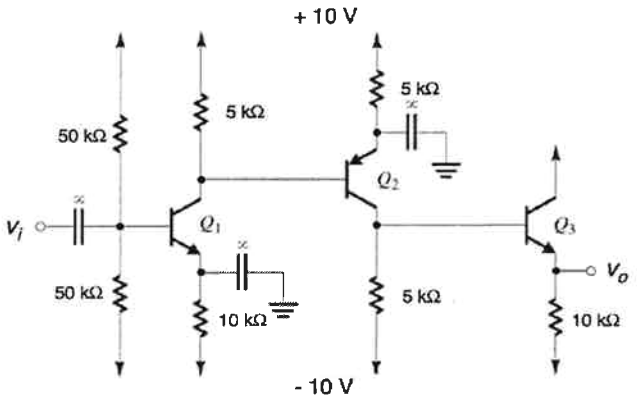
(f) Sketch and clearly label the breakpoints of the inverter voltage transfer characteristic. Identify the reference voltage V_R on the plot.

▶ **[3 points]**



▼ *Question 3:*

The circuit on the left shows a circuit for a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.



Assume $|V_{BE}| = 0.7$ V, β=100 and neglect Early effect.

Also, neglect the base current in all DC bias calculations.

► **Answer the following questions.**

(a) Find the dc bias current in each of the three transistors.

► **[2 points]**

(b) Determine the transconductance g_m of each transistor shown in the circuit.

► **[1 point]**

(c) Find the input and output resistance.

► **[2 points]**

(d) Compute the overall voltage gain v_o/v_i.

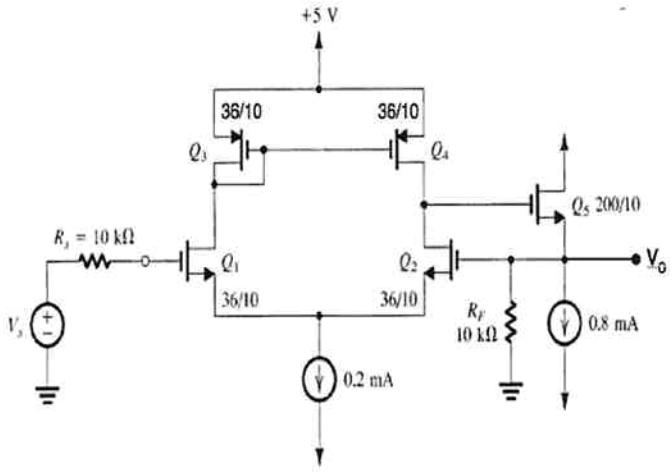
► **[3 points]**

(e) Find the frequency of the high-frequency pole formed at the interface between the first and second stages. Assume that $C_{\mu 2}$=1 pF and $C_{\pi 2}$=12 pF.

▶ [2 points]

Question 4:

(a) Assuming a single-loop negative feedback system, determine the corresponding parameters A, β and α for the following circuit. Assume the device lambda's are all equal to 0.1 with process parameter μC_{OX}=100 $\mu A/V^2$.



Draw the corresponding block diagram for this amplifier. Identify in the circuit to the right the location of the error signal used in your analysis.

▶ [5 points]

(b) What effect does a 10% change in the feedfoward amplifier gain found in part (a) have on the closed loop gain of the amplifier? How about a -20% change in the feedforward gain? Please quantify.

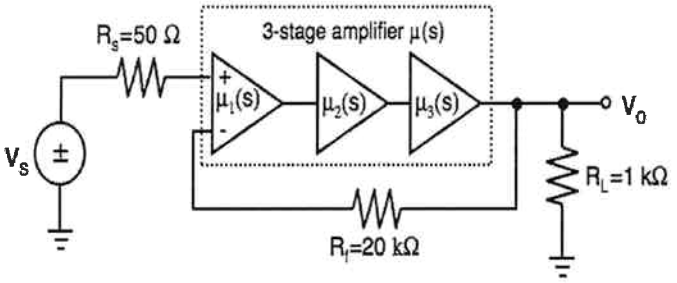
▶ **[3 points]**

(c) What effect does a 10% change in the feedback gain have on the closed loop gain of the amplifier? Please quantify.

► **[2 points]**

▼ *Question 5:*

Consider the 3-stage amplifier connected with negative feedback as shown in the figure to the right.



The transfer function $\mu(s) = \mu_1(s)\,\mu_2(s)\mu_3(s)$, where $\mu_1(s)$, $\mu_2(s)$, and $\mu_3(s)$ are all voltage amplifiers (voltage-in, voltage-out).

All stages $\mu_1(s)$, $\mu_2(s)$, and $\mu_3(s)$ have $R_{in} = \infty\ \Omega$ and $R_{out} = 0\ \Omega$.

$$\mu_1(s) = \frac{50}{\left(1 + s/10^9\right)}; \quad \mu_2(s) = \frac{10\left(1 - s/10^8\right)}{\left(1 + s/10^4\right)}; \quad \mu_2(s) = \frac{10}{\left(1 + s/10^9\right)};$$

▶ Answer the following questions.

(a) What is the feed-forward transfer function A(s) ?

▶ **[1 point]**

(b) What is the feedback transfer function β(s)?

▶ **[1 point]**

(c) Write an expression for the amplifier 's phase margin? Is the closed-loop amplifier stable or unstable?

► **[2 points]**

(d) Sketch a Bode plot of the amplitude and phase for the loop gain $A\beta(s)$. Identify the phase margin directly on the plot. It should correspond to the result you found in part (c).

▶ **[3 points]**

(e) Can you suggest an alternative approach to identifying the stability of the closed-loop amplifier. Provide a formula to quantify your approach.

► **[2 points]**