McGill

ECSE 304-334

Introduction To Microelectronic Circuits

Final Examination
Dec. 8, 2006
2:00 PM - 5:00 PM

Examiner: Prof. G. Roberts GR
Associate Examiner: Prof. R. Khazaha RK

Name: _____

Student No.: _____

Special Notes:

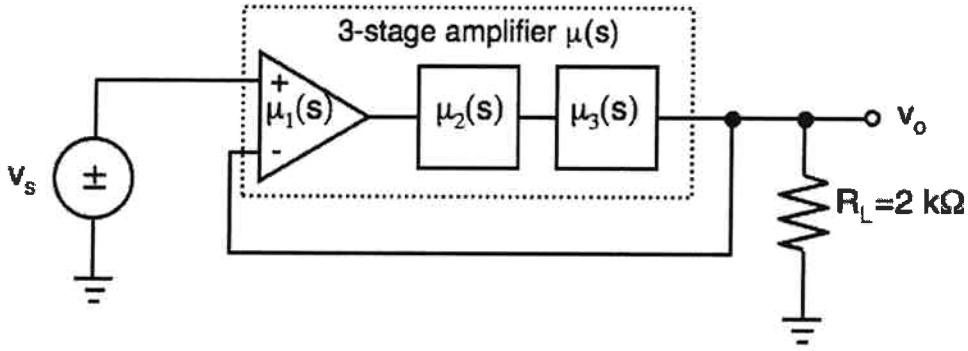
- Answer all 5 questions.
- Questions have equal weight; Distribution is indicated in brackets.
- Answer directly on the question sheet provided. You may use the back of the sheet to continue your answer.
- Only the sheets provided will be marked.
- Closed-book exam; a one-sided crib sheet is allowed.
- Write your name and student number on the top of this sheet and on the top of each of the question sheets that you want marked.
- Closed-book exam.
- Only the faculty approved calculator is permitted.

Marking Scheme:

Q1 (10 points)	*Q2 (10 points)*	*Q3 (10 points)*	*Q4 (10 points)*	*Q5 (10 points)*	*TOTAL*

Question 1:

Consider the 3-stage amplifier connected with negative feedback as shown in the figure below. The transfer function $\mu(s) = \mu_1(s)\mu_2(s)\mu_3(s)$, where $\mu_1(s)$, $\mu_2(s)$, and $\mu_3(s)$ are all voltage amplifiers (voltage-in, voltage-out).



where

$$\mu_1(s) = 50\frac{1}{1+\frac{s}{10^{11}}}; \qquad \mu_2(s) = 20\frac{\left(1-\frac{s}{10^{8}}\right)}{\left(1+\frac{s}{10^{6}}\right)\left(1+\frac{s}{10^{9}}\right)}; \qquad \mu_3(s) = 1;$$

All stages $\mu_1(s)$, $\mu_2(s)$, and $\mu_3(s)$ have $R_{in} = \infty\ \Omega$ and $R_{out} = 0\ \Omega$. Answer the following questions:

(a) What is the feed-forward transfer function A(s) ? **(1 point)**

(b) What is the feedback transfer function β(s)? **(1 point)**

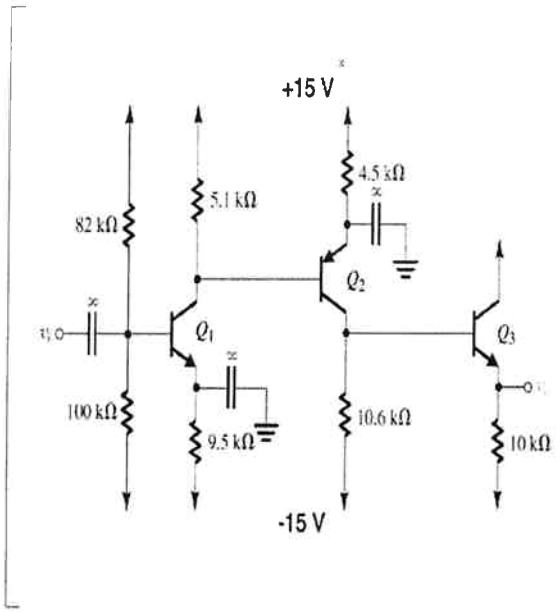
(c) Write an expression for the amplifier 's phase margin? Is the closed-loop amplifier stable or unstable?

(3points)

(d) Sketch a Bode plot of the amplitude and phase for the loop gain $A\beta(s)$. Identify the phase margin directly on the plot. **(3 points)**

(e) It is decided to replace $\mu_3(s)$ with a single time constant circuit having a transfer function $\mu_3(s) = 1$ $(1+s/\omega_o)$ such that ω_o shall be the new dominant pole of the 3-stage amplifier $\mu(s)$. Select the pole frequency ω_o such that the closed loop amplifier will be stable with a phase margin of at least 45 degrees? **(2 points)**

Question 2:



The circuit on the left shows a circuit for a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest. Assume $|V_{BE}| =$ 0.7 V, β=100 and neglect Early effect. Also, neglect the base current in all DC bias calculations.

(a) Find the dc bias current in each of the three transistors. **(2 points)**.

(b) Determine the transconductance g_m of each transistor shown in the circuit. **(1 point)**

(c) Find the input and output resistance of the amplfier circuit. **(2 points)**

(d) Compute the overall voltage gain v_o/v_i. **(3 points)**

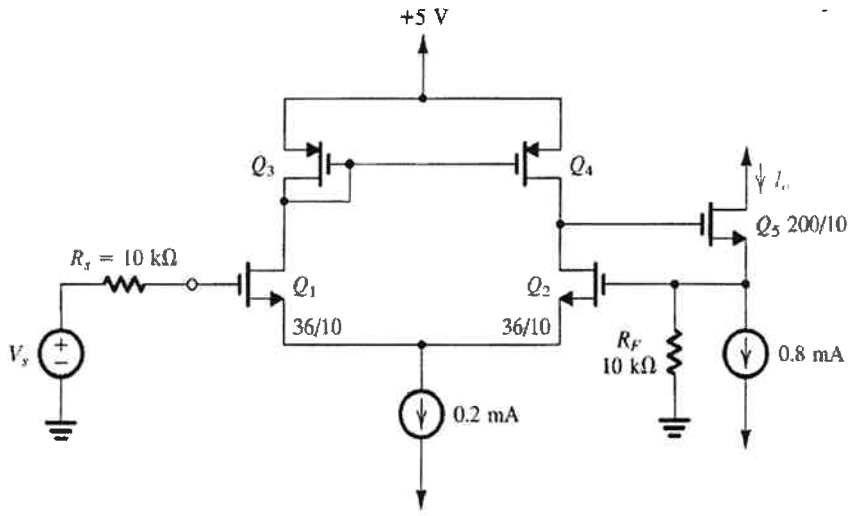
(e) Find the frequency of the high-frequency pole formed at the interface between the first and second stages. Assume that $C_{\mu 2}$=1 pF and $C_{\pi 2}$=12 pF. **(2 points)**

Question 3:

(a) Draw the block diagram of a single-loop negative feedback system. Label critical signals and write a set of equations that describe it's operation. **(2 points)**

(b) What is the priminary purpose of using negative feedback for amplfiier design? What is the potential drawback of such a scheme? **(2 points)**

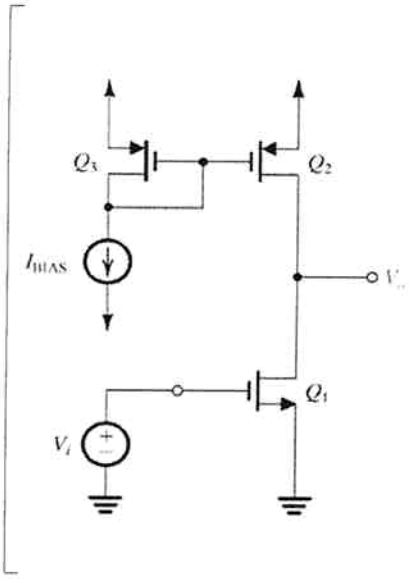
(c) Assuming a single-loop negative feedback system, determine the corresponding parameters A, β and α, and its product Aβ for the following circuit. Assume the device lambda's are all equal to 0.1 with process parameter μC_{OX}=100 μA/V^2. Draw the corresponding block diagram for this amplifier. Identify in the circuit below the location of the error signal used in your analysis. **(5 points)**



(c) continued

(d) What is the closed-loop gain Af? **(1 point)**

Question 4:



It is required to analyze the high-frequency response of the CMOS amplifier shown to the left. The DC bias current is set to 50 μA.

For Q_1,

$\mu_n C_{OX}$=100 μA/V^2,
V_A=15 V,
W/L = 100 μm/2 μm
C_{gs}=0.2 pF
C_{gd}= 0.015 pF
C_{db}=20 fF

For Q_2 and Q_3,

$\mu_p C_{OX}$=40 μA/V^2,
$|V_A|$=20 V
W/L = 20 μm/2 μm
C_{gs}=0.2 pF
C_{gd}= 0.015 pF
C_{db}=20 fF

Assume that the source resistance of the input signal generator is 50 ohms . Also, for simplicity assume that the signal voltage at the gate of Q_2 is zero.

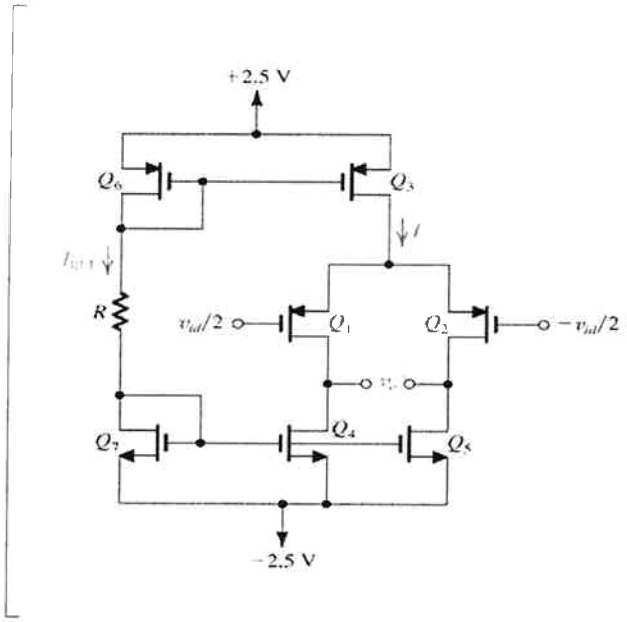
Based on the information given above, find:

(a) Low-frequency voltage gain. **(4 points)**

(b) Estimate the 3-dB frequency. State clearly the method used. **(6 points)**

(b) continued .....

Question 5:



The circuit on the left shows a circuit for a differential amplifier with an active load. Here Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2, respectively.

The dc bias circuit that establishes the appropirate dc voltage at the drains of Q_1 and Q_2 is not shown.

The technology avaliable is described as follows:

$\mu_n C_{OX}=100\ \mu A/V^2$,
$\mu_p C_{OX}=40\ \mu A/V^2$,
$V_{tn}=|V_{tp}|=0.5V$,
$V_{An}=20$ V,
$|V_{Ap}|=20$ V.

Design the circuit above such that the following specifications are met:

(i) Differential gain $A_d=100$ V/V.
(ii) $I_{REF}=I=100\ \mu A$.
(iii) The dc voltage at the gate of Q_6 and Q_3 is +1.2 V.
(iv) The dc voltage at the gate of Q_7, Q_4 and Q_5 is -1.2 V.

Specify the value of R and the W/L ratios for the 7 MOS transistors **(8 points + 2 points for presentation)**. For dc bias calculations, you may neglect channel-length modulation effects.

Question 5 continued .....

Question 5 continued .....