McGill University
Faculty of Engineering

Introduction to Microelectronics
Final Examination - Fall 2004

Course no.: ECSE 334 A

Friday December 10th, 2003

14:00 - 17:00 (3 Hours)

Examiner: Prof. Mourad El-Gamal

Co-Examiner: Prof. Anas Hamoui Anas Hamoui

Student Last Name:_____

Student First Name:_____

McGill ID Number: _____

- Answer **ALL QUESTIONS** **on the exam booklet** provided.
- Please make sure to **fill and hand in back** with your exam booklet the **summary table of answers** sheet attached at the end of this exam. Points will be deducted for every missing entry in this table.
- Points distribution is indicated between brackets, when applicable.
- Do not forget to write your name and student ID number on the top of this sheet.
- This is a closed-book exam.
- Only the faculty supported calculators are permitted.
- Make sure you have a **total of 9 pages** (including this one) **BEFORE** you start.
- State any assumptions you find *necessary* to complete your answer.

Good Luck !

Question #	1	2	3	4	TOTAL
Mark					/ 100
Total Points	30	20	30	20	100

According to McGill's Code of Student Conduct and Disciplinary Procedures, plagiarism is an academic offence. Appropriate actions will be taken to deal with students who are found violating the Code, and they will be reported to the Associate Dean.

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QUESTION 1 - MULTI-STAGE AMPLIFIERS: [Total points 30]

Figure 1 shows the circuit of a CMOS operational amplifier. All MOS devices have $|V_t| = 1$ V, $\mu_n C_{ox} = 2\mu_p C_{ox} = 40\ \mu A/V^2$, $|V_A| = 50$ V, and $L = 5\ \mu m$. Device widths are indicated on the diagram as multiples of W, where $W = 5\ \mu m$.

1.1- **[2 points]** Design R to provide a 10-μA reference current I_{REF}.

1.2- **[4 points]** Assuming $v_o = 0$ V, as established by external feedback, perform a bias analysis, finding all the labeled node voltages.

1.3- **[5.2 points]** Provide in table format I_D, V_{GS}, g_m, and r_o for all devices.

1.4- **[6.8 points]** Calculate the voltage gain $A_v = v_o / (v_+ - v_-)$, the differential input resistance R_{indiff}, and the output resistance R_{out}.

1.5- **[3 points]** What is the input common-mode range (ICMR) ?

1.6- **[3 points]** What is the output signal range for no load ?

1.7- **[3 points]** For what load resistance R_{load} connected to ground is the minimum output voltage limited to -1 V before Q_7 begins to conduct ?

1.8- **[3 points]** For a load resistance one-tenth of that found in part 1.7, what is the output signal swing ?

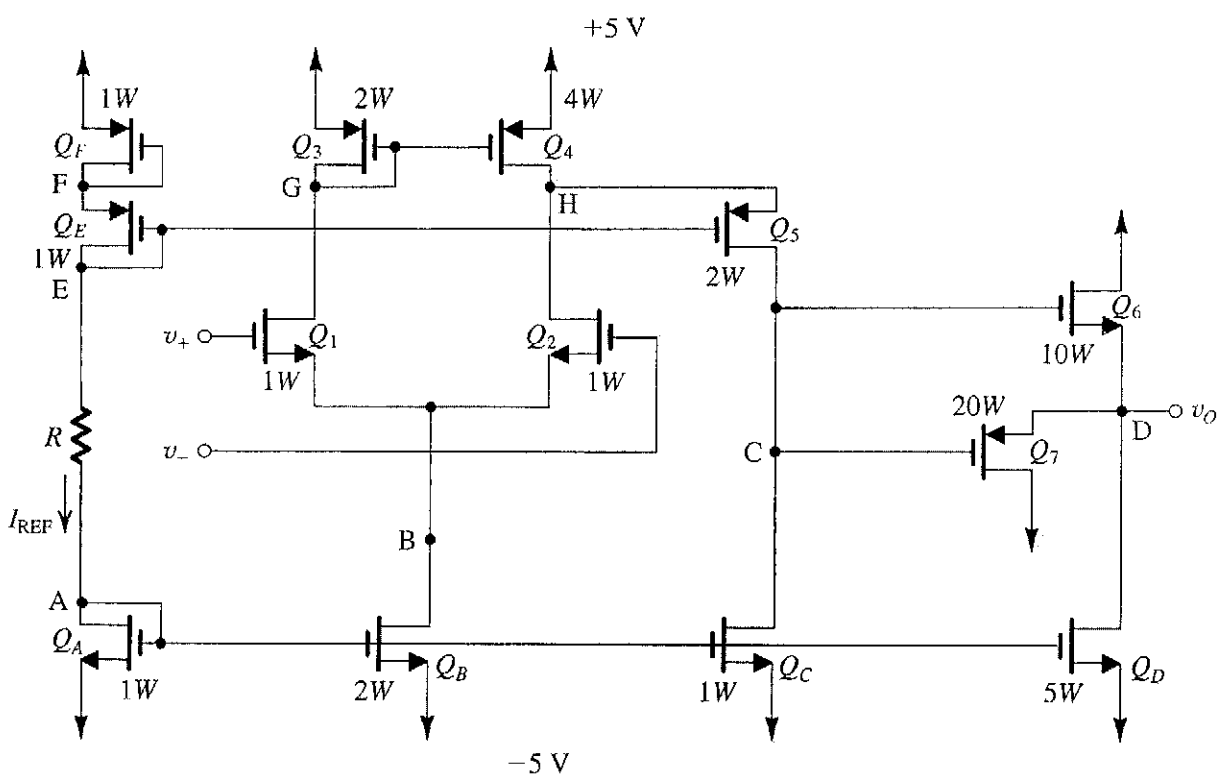

Figure 1.

QUESTION 2 - OUTPUT STAGES: [Total points 20]

The BiCMOS follower shown in Figure 2 uses devices for which $V_{BE} = 0.7$ V, $V_{CEsat} = 0.3$ V, $\mu_n C_{ox} W/L = 20$ mA/V^2, and $V_t = -2$ V.

2.1- **[5 points]** For linear operation, what is the range of output voltages obtained with R_L = infinity ?

2.2- **[5 points]** For linear operation, what is the range of output voltages obtained with $R_L = 100\ \Omega$?

2.3- **[5 points]** What is the smallest load resistor allowed for which a 1-V peak sine-wave output is available ?

2.4- **[5 points]** What is the corresponding power conversion efficiency ?

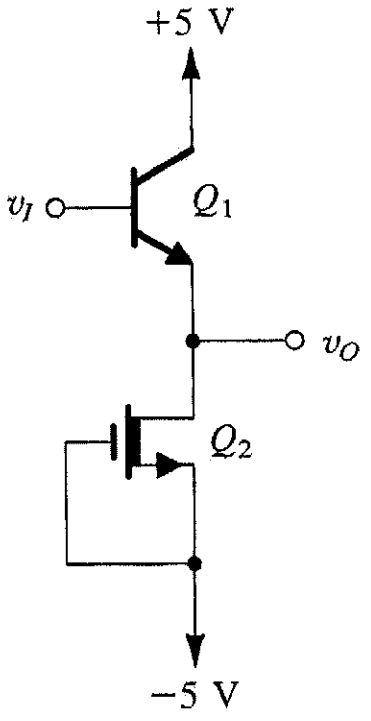

Figure 2.

QUESTION 4 - STABILITY: [Total points 20]

Consider an op amp with an open-loop voltage gain of 80 dB and poles at 10^5 Hz, 10^6 Hz, and 2×10^6 Hz is to be compensated to be stable for unity gain feedback (i.e. β=1). Assume that the op-amp incorporates an amplifier equivalent to that in Figure 4, with $C_1 = 150$ pF, $C_2 = 5$ pF, and $g_m = 40$ mA/V, and that the pole at f_{P1} is caused by the input circuit, and that the pole at f_{P2} is introduced by the output circuit of this amplifier. Find the value of the required compensating Miller capacitance C_f, and the new frequency of the output pole.

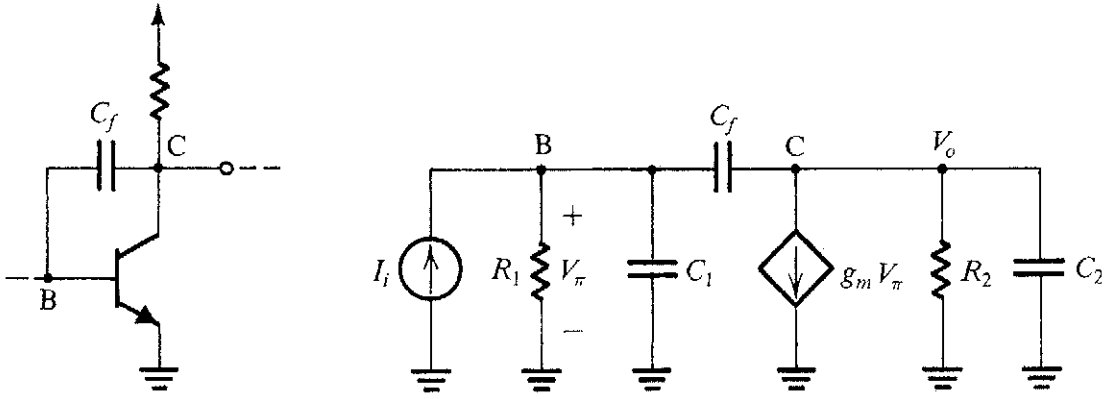

Figure 4.

QUESTION 3 - FEEDBACK: [Total points 30]

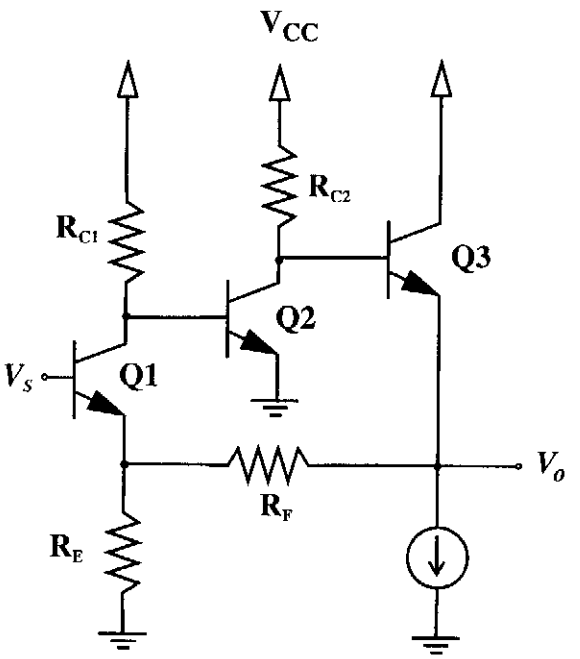

Figure 3.

Figure 3 shows a series-shunt feedback amplifier without the details of the bias circuit.

3.1. [9 points] Find expressions for the open-loop gain A, the feedback factor β, and the preprocessing stage α. Draw the resulting Signal Flow Graph (SFG).

3.2. [3 points] Show that if $A\beta$ is large, then the closed-loop voltage gain is given approximately by

$$A_f \equiv \frac{V_o}{V_S} \cong \frac{R_F + R_E}{R_E}$$

3.3. [3 points] If R_E is selected equal to 50 Ω, find R_F that will result in a closed-loop gain of approximately 25 V/V.

3.4. [6 points] If Q1 is biased at 1 mA, Q2 at 2 mA, and Q3 at 5 mA, and assuming the transistors have $h_{fe} = 100$, find approximate values for R_{C1} and R_{C2} to obtain gains from the stages of the A-circuit as follows: a voltage gain from Q1 of about -10 V/V and a voltage gain from Q2 of about -50 V/V.

3.5. [3 point] For your design, what is the closed-loop voltage gain realized ?

3.6. [6 points] Calculate the input and output resistances of the closed-loop amplifier designed.

Table 4.2 SUMMARY OF THE BJT CURRENT–VOLTAGE RELATIONSHIPS IN THE ACTIVE MODE

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1 - \alpha) i_E = \frac{i_E}{\beta + 1}$$

$$i_C = \beta i_B \qquad i_E = (\beta + 1) i_B$$

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1}$$

V_T = thermal voltage $= \dfrac{kT}{q} \cong 25$ mV at room temperature

Table 4.3 RELATIONSHIPS BETWEEN THE SMALL-SIGNAL MODEL PARAMETERS OF THE BJT

Model Parameters in Terms of DC Bias Currents:

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right)$$

$$r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{V_A}{I_C}$$

In terms of g_m:

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In terms of r_e:

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta + 1) r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between α and β:

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1} \qquad \beta + 1 = \frac{1}{1 - \alpha}$$

Current-Voltage Relationships

■ For NMOS Devices:

- *Triode region* ($v_{GS} \geq V_t$, $v_{DS} \leq v_{GS} - V_t$)

$$i_D = k'_n \left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

For small v_{DS}: $r_{DS} \equiv \dfrac{v_{DS}}{i_D} = \left[k'_n\left(\dfrac{W}{L}\right)(v_{GS} - V_t)\right]^{-1}$

- *Saturation region* ($v_{GS} \geq V_t$, $v_{DS} \geq v_{GS} - V_t$)

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

- $k'_n = \mu_n C_{ox}$ (see Table 5.1)

$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right]$

$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}$, $q = 1.6 \times 10^{-19}$ coulomb, $\varepsilon_s = 1.04 \times 10^{-12}$ F/cm

$\lambda = 1/V_A$, $V_A \propto L$

■ For PMOS Devices: V_t, γ, λ and V_A are negative

- For triode region, $v_{GS} \leq V_t$ and $v_{DS} \geq v_{GS} - V_t$
- For saturation region, $v_{GS} \leq V_t$ and $v_{DS} \leq v_{GS} - V_t$

■ For Depletion Devices (refer to Fig. 5.23):

- n channel: V_t is negative
- p channel: V_t is positive
- $I_{DSS} = \dfrac{1}{2}k'\left(\dfrac{W}{L}\right)V_t^2$

Small-Signal Model (Fig. 5.67)

$$g_m = \sqrt{2k'(W/L)}\sqrt{I_D} \qquad r_o = \frac{|V_A|}{I_D}$$

$$g_m = k'(W/L)(V_{GS} - V_t)$$

$$g_m = \frac{2I_D}{V_{GS} - V_t} \qquad V_{GS} - V_t \equiv V_{eff}$$

$$g_{mb} = \chi g_m, \qquad \chi = \gamma/[2\sqrt{2\phi_f + |V_{SB}|}]$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} \qquad C_{gd} = WL_{ov}C_{ox}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \dfrac{|V_{SB}|}{V_0}}} \qquad C_{db} = \frac{C_{db0}}{\sqrt{1 + \dfrac{|V_{DB}|}{V_0}}}$$

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Last Name:

First name:

ID Number:

Question Number		Value
1.1	*Biasing R*	
1.2	V_A	
	V_B	
	V_C	
	V_D	
	V_E	
	V_F	
	V_G	
	V_H	

Question Number		I_D (μA)	V_{GS} (V)	g_m (μA/V)	r_o (MΩ)
1.3	Q_1				
	Q_2				
	Q_3				
	Q_4				
	Q_5				
	Q_6				
	Q_7				
	Q_A				
	Q_B				
	Q_C				
	Q_D				
	Q_E				
	Q_F				

Question Number		Value
1.4	$A_v = v_o / (v_+ - v_-)$	
	R_{indiff}	
	R_{out}	
1.5	ICMR	$v_{ICM\text{-}max}$ = ; $v_{ICM\text{-}min}$ =
1.6	Output range for no load	$v_{out\text{-}max}$ = ; $v_{out\text{-}min}$ =
1.7	R_{load}	
1.8	Output signal swing	$v_{out\text{-}max}$ = ; $v_{out\text{-}min}$ =

Last Name: **ID Number:**

First name:

Question Number		Value
2.1	Output range (R_L = infinity)	$v_{out\text{-}max}$ = ; $v_{out\text{-}min}$ =
2.2	Output range (R_L = 100 Ω)	$v_{out\text{-}max}$ = ; $v_{out\text{-}min}$ =
2.3	Smallest R_L for a 1-V peak output	
2.4	Power efficiency	

Question Number		Value
3.1		Answer in booklet only
3.2		Answer in booklet only
3.3	R_F for 25 V/V loop gain	
3.4	R_{C1}	
	R_{C2}	
3.5	Closed loop voltage gain	
3.6	Input resistance of closed loop	
	Output resistance of closed loop	

Question Number		Value
4.1	Miller compensating capacitance	
4.2	New frequency of the output pole	