McGill University -

Faculty of Engineering

Department of Electrical and Computer Engineering

ECSE 334 - Introduction to Microelectronics
Final Examination (April 11, 2006)
3 hours (2:00PM-5:00PM)

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Co-Examiner: Prof. Mourad N. El-Gamal

❑ INSTRUCTIONS/NOTES:

- This is a closed-book examination. Only the faculty-approved calculators are permitted.
- The examination includes 3 questions and consists of 9 pages, including this cover page.
- A summary of the BJT and MOSFET characteristics is attached (4 pages).
- Make sure you have total of 13 pages, BEFORE you start solving this examination.
- **All questions have equal weight.**
- State any assumptions you find *necessary* to complete your answers.
- For full credit, you must show the **steps** you followed to answer the questions and you must clearly indicate the **units** in your answers.
- **Answer all questions in the exam books provided. Underline your answers.**
- Write your name on this cover page and on top of each question which you want marked. Place the sheets which you want to be marked inside your exam booklet.
- **Return ALL pages of this of this examination to the Invigilator.**
  You are NOT allowed to leave this room with any examination paper.

Student Last Name: _____

Student First Name: _____

McGill Student ID: _____

Question #	1	2	3	4	Total
Mark	/25	/25	25	/25	/100

DEVICE PARAMETERS

- **MOSFET Parameters:**

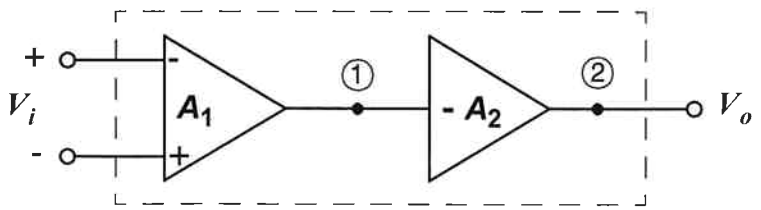
For a MOSFET in the saturation region and having $L = 0.5\mu m$:

	NMOS Transistor	PMOS Transistor
$\|V_{t0}\|$	0.6 V	0.65 V
λ	0.25 V^{-1}	0.40 V^{-1}
μC_{ox}	200 $\mu A/V^2$	50 $\mu A/V^2$
C_{ox}	5 $fF/\mu m^2$	5 $fF/\mu m^2$
$L_{ov}C_{ox}$	0.625 $fF/\mu m$	0.625 $fF/\mu m$

- **BJT Parameters:**

	npn BJT	pnp BJT
$\|V_{BEon}\|$	0.7 V	0.7 V
$\|V_{BCon}\|$	0.4 V	0.4 V
$\|V_{CEsat}\|$	0.3 V	0.3 V
$\beta = h_{fe}$	120	50
C_μ	5 fF	15 fF
r_x	400 Ω	200 Ω
$\|V_A\|$	35 V	30 V
V_T	25 mV	25 mV

- **Note:** $1\ fF = 10^{-3}\ pF = 10^{-15}\ F$



Two-Stage Opamp

Figure 1

Question 1: Frequency Compensation [25 marks]

Consider the two-stage opamp shown in Figure 1.

Its open-loop transfer function $A(s) = V_o(s)/V_i(s)$ has:

- a dc gain of $A_0 = A_1A_2 = 60\,\text{dB}$;
- poles at $f_{p1} = 1\,\text{MHz}$, $f_{p2} = 10\,\text{MHz}$, and $f_{p3} = 100\,\text{MHz}$.

The 1st pole (at f_{p1}) is formed at node 1 and the 2nd pole (at f_{p2}) is formed at node 2.

The total capacitance at node 1 is $C_1 = 7\,\text{pF}$.

The dc gains of the individual stages are $A_1 = 50\,\text{V/V}$ and $A_2 = 20\,\text{V/V}$.

The opamp is to be connected in a negative-feedback loop via a feedback network whose feedback factor B is frequency independent.

It is required to compensate the opamp, so that it is stable with a phase margin of $\boldsymbol{PM = 45^o}$ for a feedback factor $\boldsymbol{B = 1}$.

Consider the following 3 compensation schemes:

a) Compensation Scheme 1: the opamp is compensated by introducing a new dominant pole.

- Find the frequency f_D at which the new pole must be placed.

b) Compensation Scheme 2: the opamp is compensated by placing an additional capacitance C_C at node 1 to reduce the frequency of the 1st pole.

- Find the frequency f_{p1}' to which the 1st pole must be shifted. Assume that the frequencies of the other poles remain unchanged.
- Find the required size for capacitor C_C.

c) Compensation Scheme 3: the opamp is to be compensated by connecting a compensating capacitor C_C between nodes 1 and 2.

- Find the frequency f_{p1}' to which the 1st pole must be shifted. Assume that such frequency compensation will also shift the 2nd pole (at f_{p2}) to a frequency $f_{p2}' >> f_{p3}$.
- Find the required size for capacitor C_C.

Specifications

$R_S = 5\ k\Omega$

$R_F = 5\ k\Omega$

$R_L = 2\ k\Omega$

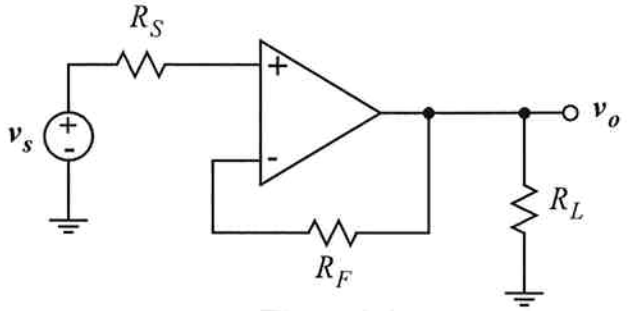


Figure 2 (a)

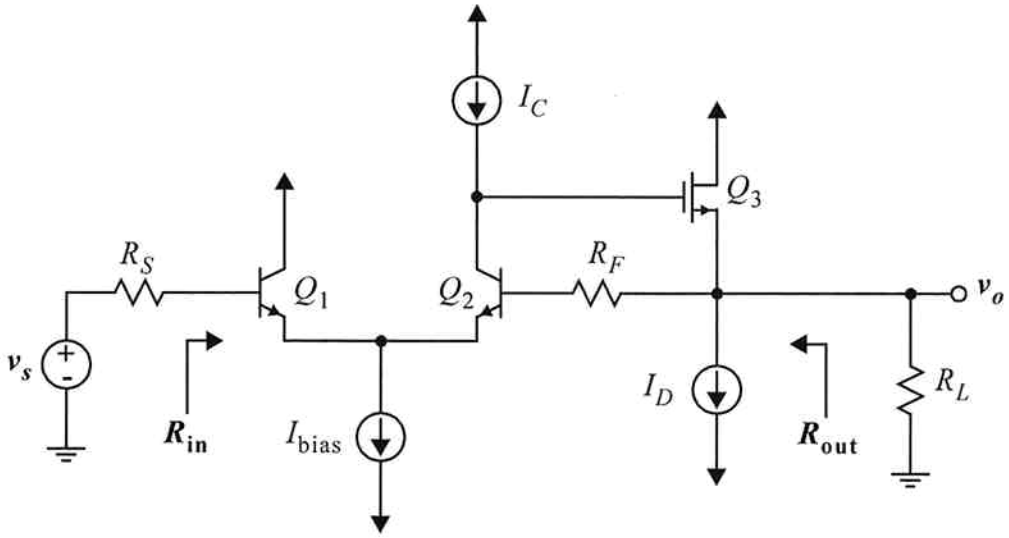


Figure 2 (b)

Question 2: Feedback Amplifiers [25 marks]

The series-shunt feedback amplifier in Figure 2(a) is implemented as shown in Figure 2(b). Assume that:

- the signal source v_s has a **dc** component of 0 V and the bias voltage level at the output is stabilized by feedback to about 0 V;
- the **dc** base currents of the BJTs are negligible;
- current source I_{bias} is ideal;
- the incremental output resistances of sources I_C and I_D are R_c and R_d, respectively.

For simplicity, write your expressions using the variables previously derived, together with the BJT small-signal parameters, the incremental output resistance of the current sources (R_c,R_d), and the external resistors (R_S, R_F, R_L).

Refer to the β of the BJT as h_{fe}. Use subscripts to associate each small-signal parameter with its corresponding transistor number.

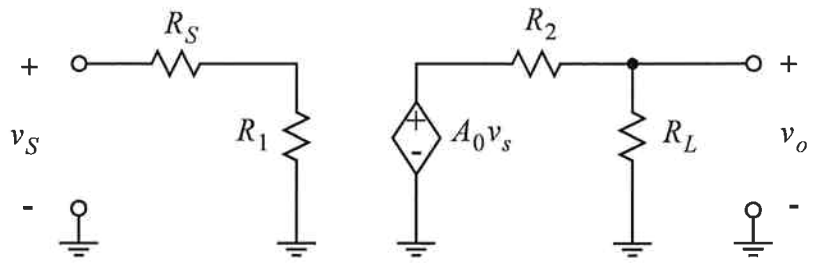


Figure 2 (c)

a) Use feedback analysis to write the expression for:

- **i)** the feedback factor B
- **ii)** the open-loop gain A
- **iii)** the closed-loop gain $A_f \equiv v_o / v_s$
- **iv)** the input resistance R_{in}
- **v)** the output resistance R_{out}

of the feedback amplifier in Figure 2(b).

b) Write the expression for

- R_1
- R_2
- A_0

in Figure 2(c), such that the voltage amplifier model in Figure 2(c) is equivalent to the feedback amplifier circuit in Figure 2(b).

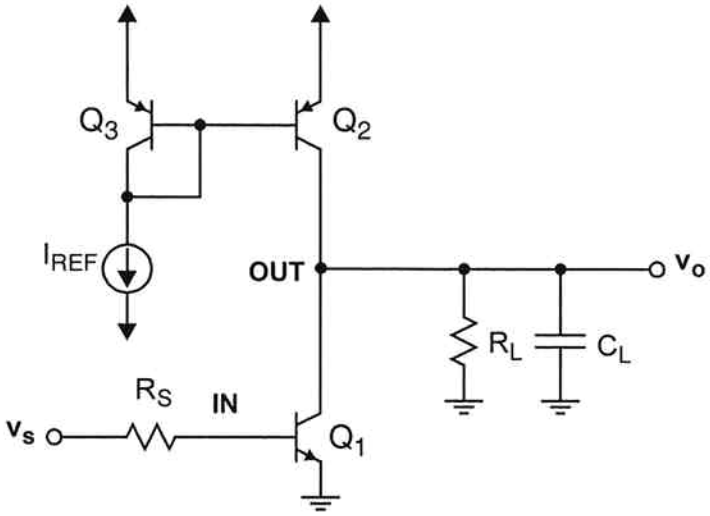


Figure 3 (a)

Question 3: High-Frequency Response [25 marks]

Consider the active-loaded common-emitter (CE) amplifier in Figure 3(a).

In the following, assume that:

- all BJTs are biased in the active region;
- **the signal voltage at the base of transistors Q2 and Q3 is zero.**

Do NOT neglect r_x in the BJT small-signal models.

For simplicity, write your expressions using the variables previously derived, together with the BJT small-signal parameters. **Use subscripts to associate each small-signal parameter with its corresponding transistor number.**

a) For the CE amplifier in Figure 3(a), write the expression for:

- its midband gain $A_{Ma}=v_o/v_s$;
- its 3-dB frequency ω_{Ha}, assuming a dominant pole is formed at node IN.

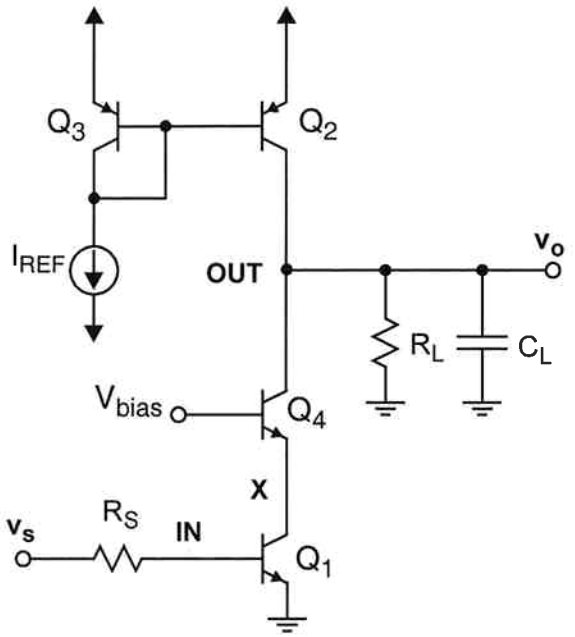


Figure 3 (b)

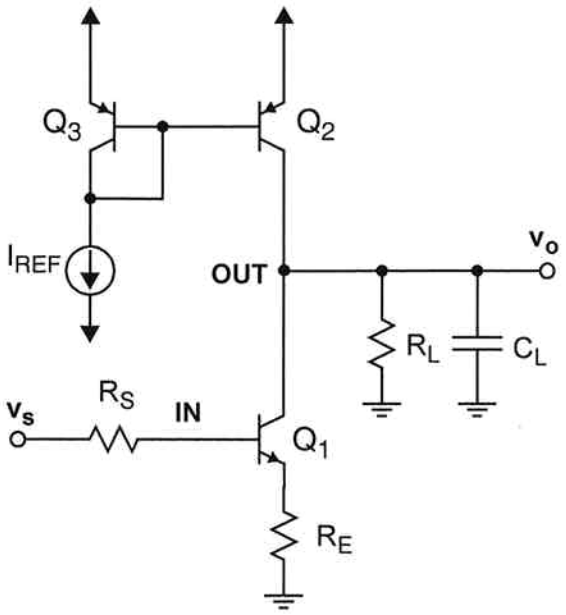


Figure 3 (c)

b) To increase the 3-dB frequency of the CE amplifier in Figure 3(a), a common-base transistor $Q4$ is placed at the collector of $Q1$, as shown in Figure 3(b).

For the cascode amplifier in Figure 3(b), write the expression for:

- its midband gain $A_{Mb}=v_o/v_s$;
- the high-frequency pole ω_{INb} associated with node IN;
- the high-frequency pole ω_{Xb} associated with node X
- the high-frequency pole ω_{OUTb} associated with node OUT.

c) To increase the input resistance of the CE amplifier in Figure 3(a), a resistor R_E is placed in the emitter of $Q1$, as shown in Figure 3(c).

For the CE amplifier in Figure 3(c), write the expression for:

- its midband gain $A_{Mc}=v_o/v_s$;
- its 3-dB frequency ω_{Hc}, assuming a dominant pole is formed at node IN.

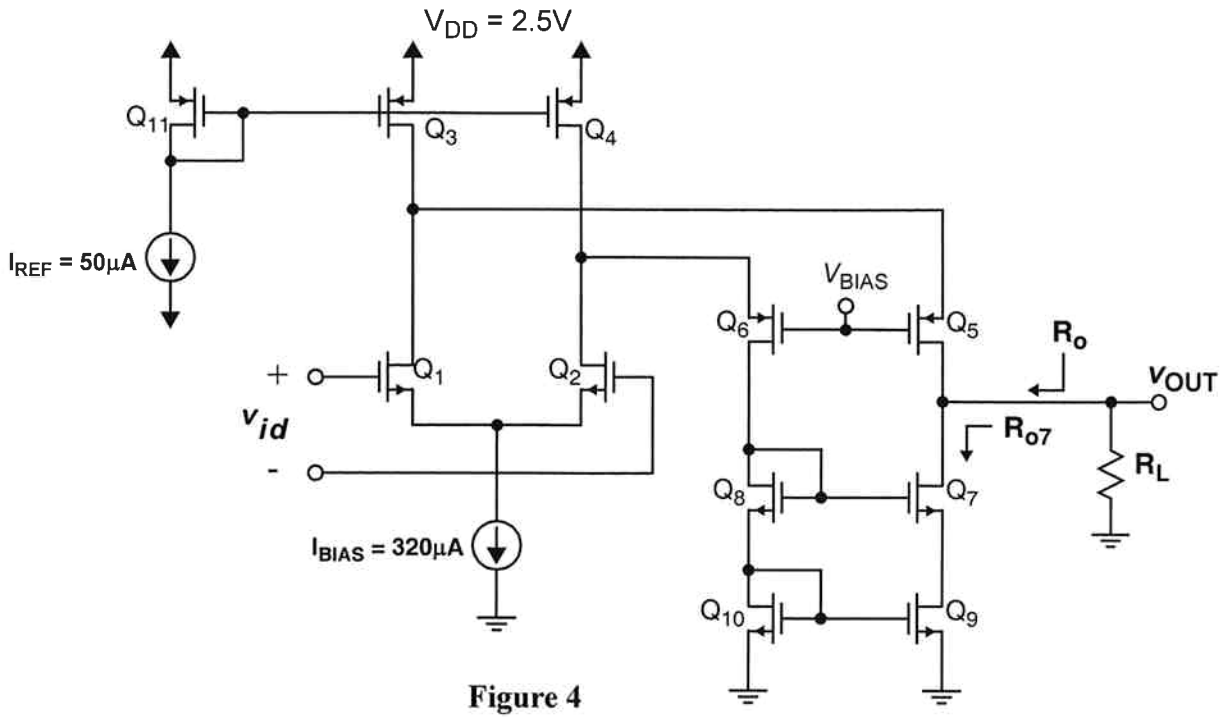


Figure 4

Question 4: Differential and Cascode Amplifiers [25 marks]

Figure 4 shows a folded-cascode differential CMOS opamp.

The MOSFET parameters are listed on page 2. Ignore the body effect.

Assume that:

- $\gamma = 0$ and $\lambda = 0$ in your dc calculations;
- all MOSFETs are biased in the saturation region and operate at $|V_{OV}| = 0.25$ V;

For simplicity, write your expressions using the variables previously derived, together with the MOSFET small-signal parameters. **Use subscripts to associate each small-signal parameter with its corresponding transistor number.**

a) Specify the aspect ratio (W/L) of transistors Q_3 and Q_4, such that the ratio of the bias input currents to the cascode currents is: $I_{D1,2}/I_{D5,6} = 4$.

b) Write the expression for the output resistance R_o.

Note: The output resistance of the cascode current mirror (Q_7-Q_{10}) is $R_{O7} \cong (g_{m7}r_{o7})\, r_{o9}$.

c) Write the expression for the short-circuit transconductance $G_m \equiv |i_{out}/v_{id}|\big|_{R_L=0}$ and draw the equivalent transconductance circuit model of the opamp.

d) Write the expression for the open-circuit differential voltage gain $A_d \equiv (v_{out}/v_{id})\big|_{R_L=\infty}$.

e) Let $V_{\text{out, min}}$ denote the smallest value of output voltage V_{out} for proper operation of the CMOS opamp, with all its transistors in saturation.

- Write the expression for $V_{\text{out, min}}$. Find its value.

f) Let $V_{\text{out, max}}$ denote the largest value of output voltage V_{out} for proper operation of the CMOS opamp, with all its transistors in saturation.

- Write the expression for V_{BIAS}, which maximizes $V_{\text{out, max}}$. Find its value.
- Write the expression for the resulting $V_{\text{out, max}}$. Find its value.

SUMMARY OF BJT CHARACTERISTICS

❑ BJT Current-Voltage Relationships in the Active Mode

- For the **npn** BJT:

$$i_C = I_S\, e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

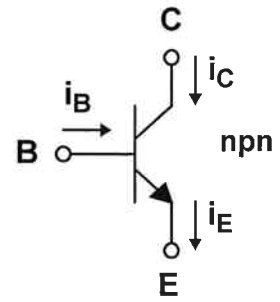
$$i_B = \frac{i_C}{\beta} = (1-\alpha)\, i_E = \frac{i_E}{\beta+1}$$

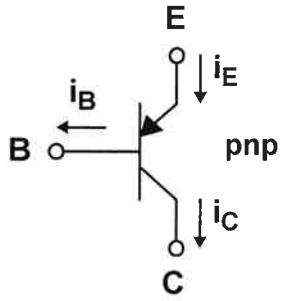
$$i_E = \frac{i_C}{\alpha} = (\beta+1)\, i_B$$

$$i_C = \alpha\, i_E = \beta\, i_B$$

$$i_E = i_B + i_C$$

where $V_T = \frac{kT}{q} \cong 25mV$ at room temperature





- For the **pnp** BJT: reverse the polarity of all terminal voltages

- Relationships between α and β:

$$\alpha = \frac{\beta}{\beta+1} \qquad \beta = \frac{\alpha}{1-\alpha} \qquad \beta + 1 = \frac{1}{1-\alpha}$$

❑ Small-Signal Equivalent Circuit Models for the BJT

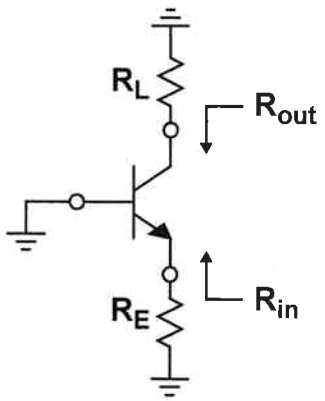
- Small-Signal Model Parameters in terms of DC Bias Currents:

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$$

- Relationships between the Small-Signal Model Parameters of the BJT:

$$g_m = \frac{\alpha}{r_e} = \frac{\beta}{r_\pi} \qquad r_\pi = (\beta+1)\, r_e \qquad \frac{1}{r_e} = g_m + \frac{1}{r_\pi}$$

Common-Base Configuration:



$$R_{\text{in}} \cong r_e\left[\frac{r_o + R_L}{r_o + R_L/(\beta+1)}\right]$$

$$R_{\text{out}} \cong r_o\left[1 + g_m(R_E \,\|\, r_\pi)\right]$$

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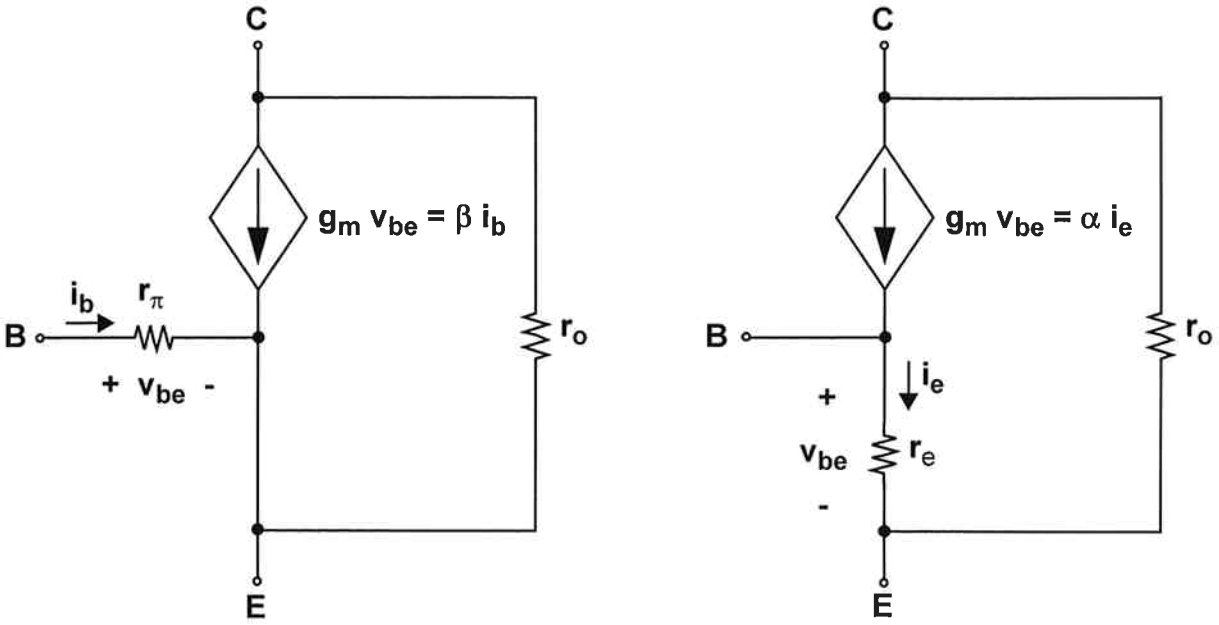
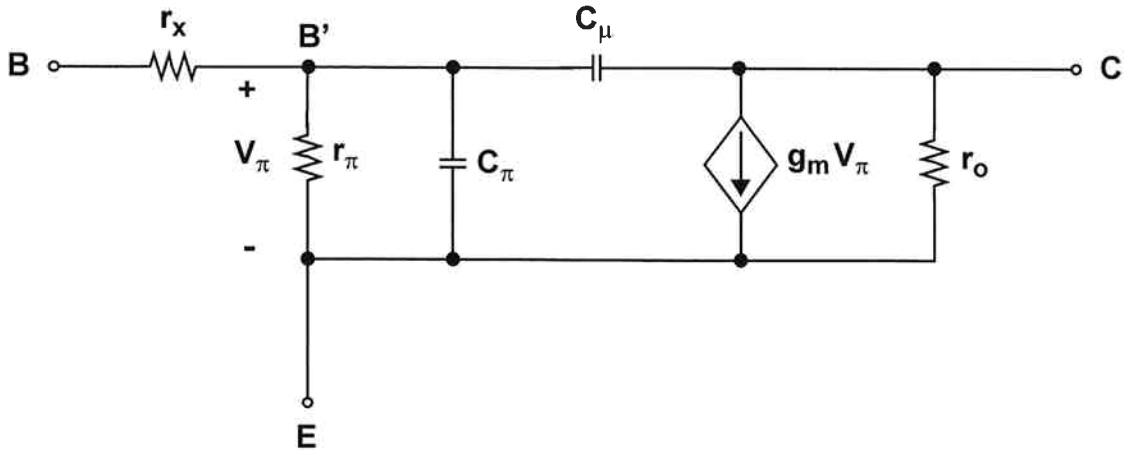
- Simplified Low-Frequency Equivalent-Circuit Models for the Small-Signal Operation of the BJT:



Hybrid-π Model **T Model**

- High-Frequency Small-Signal Model of the BJT:



SUMMARY OF MOSFET CHARACTERISTICS

Current-Voltage Relationships (Square-Law MOSFET Model)

❑ NMOS Transistor

- Overdrive (Effective) Voltage: $v_{OV} = v_{GS} - V_t$
- Triode Region: $[v_{GS} \geq V_t \Leftrightarrow v_{OV} \geq 0]$ and $[v_{GD} \geq V_t \Leftrightarrow v_{DS} \leq v_{OV}]$

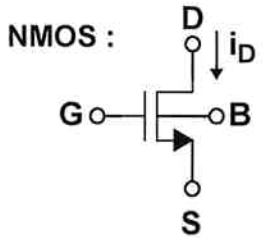
$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$$

For $v_{DS} \ll 2v_{OV}$: $\quad r_{DS} \equiv \frac{v_{DS}}{i_D} = 1/\left[\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)\right]$

- Saturation Region: $[v_{GS} \geq V_t \Leftrightarrow v_{OV} \geq 0]$ and $[v_{GD} \leq V_t \Leftrightarrow v_{DS} \geq v_{OV}]$

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

- Threshold Voltage: $V_t = V_{t0} + \gamma(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f})$

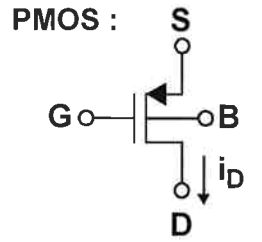


- Process Parameters:

$C_{ox} = \varepsilon_{ox}/t_{ox}$ $\quad$ (F/μm²)

$k'_n = \mu_n C_{ox}$ $\quad$ (A/V²)

$\lambda = \frac{1}{V_A} = \frac{1}{L \cdot V'_A}$ $\quad$ (V^{-1})



❑ PMOS Transistor: (V_{t0}, γ, and λ are negative)

- Reverse the polarity of all terminal voltages

and

- Exchange V_t, μ_n, λ, and k'_n with $|V_t|$, $|\lambda|$, μ_p, and k'_p, respectively.

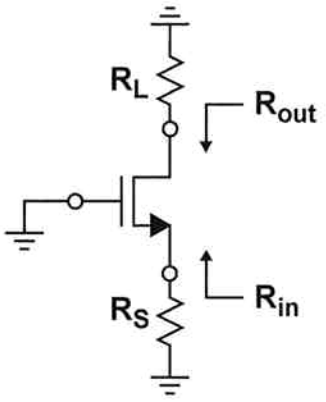
Approximation of the MOSFET Gate Capacitances (for Long-Channel MOSFETs)

Mode of Operation	C_{gb}	C_{gs}	C_{gd}
Cutoff	WLC_{ox}	0	0
Triode	0	$\frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$	$\frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$
Saturation	0	$\frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$	$WL_{ov}C_{ox}$

Small-Signal Equivalent Circuit Models for the MOSFET:

- $g_m = \mu_n C_{ox}\frac{W}{L}V_{OV} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{OV}}$
- $g_{mb} = \frac{\gamma}{2\sqrt{2\phi_F + |V_{SB}|}}g_m$
- $r_o = 1/|\lambda I_D|$
- $C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$ and $C_{gd} = WL_{ov}C_{ox}$
- $C_{db} = \frac{C_{db0}}{\left(1 + \frac{|V_{DB}|}{V_0}\right)^m}$

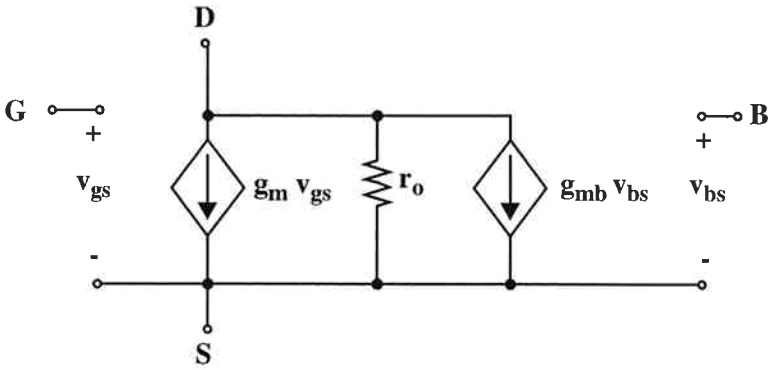
Common-Gate Configuration:



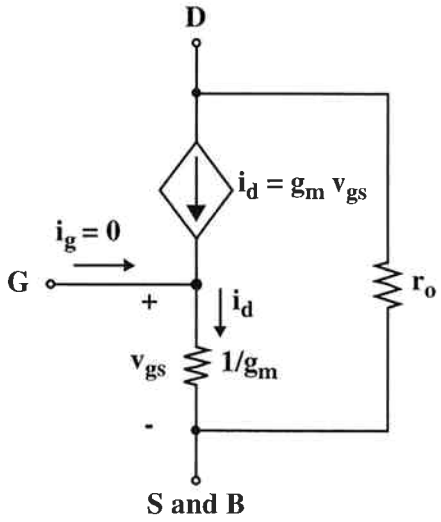
$$R_{in} \cong \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_L}{r_o}\right)$$

$$R_{out} \cong R_S + r_o[1 + (g_m + g_{mb})R_S]$$

- **Low-Frequency Small-Signal Models for the MOSFET:**

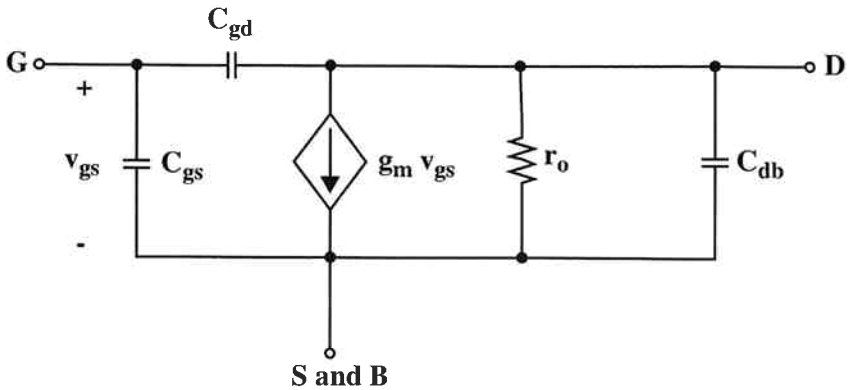


Hybrid-π Model



T model when $|V_{SB}| = 0$

- **High-Frequency Small-Signal Model for the MOSFET with no body effect ($|V_{SB}| = 0$):**



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