McGill University - Department of Electrical and Computer Engineering

ECSE 334 - Introduction to Microelectronics

Midterm

March 19, 2009, 5:35PM-7:25PM

❑ MOSFET Parameters: For a MOSFET in the saturation region and having $L = 0.5\mu m$,

- NMOS transistor: $V_{t0} = 0.6V$, $\lambda = 0.25V^{-1}$, $\mu_n C_{ox} = 200\mu A/V^2$.
- PMOS transistor: $|V_{t0}| = 0.65V$, $|\lambda| = 0.4V^{-1}$, $\mu_p C_{ox} = 50\mu A/V^2$.

❑ **NOTES:**

- This is a closed-book midterm.
- A summary of the MOSFET characteristics is attached.
- This midterm includes 2 questions and consists of 5 pages, including this cover page.
- All questions have equal weight.
- Answer all questions in the exam books provided.
  Underline your answers.
- State any assumptions you find *necessary* to complete your answers.
- Only the faculty-approved calculators are permitted.
- Write your name on top of this sheet and on top of each sheet of the question sheets that you want marked. Place the sheets that you want to be marked inside you exam booklet.
- **Return the sheets that you do not want to be marked to the invigilator for shredding.**
- Do not forget to write your name and student ID on the top of ALL pages following this sheet.

Name: ____ **SOLUTION**

Student ID:_____

Question	Mark
1	/30
2	/30
Total	/60

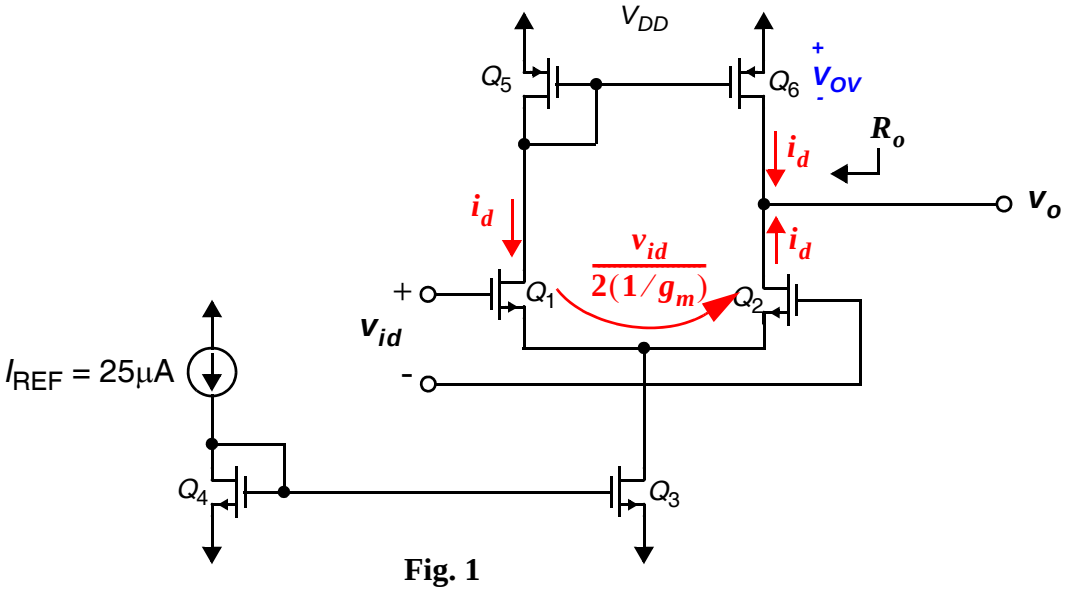

Fig. 1

Question 1: [30 marks]

Consider the CMOS differential amplifier circuit shown in Fig. 1.
Assume all MOSFETs are biased in the saturation region and have a channel length $L = 0.5\,\mu m$.
The MOSFET parameters are listed on the cover page. Ignore the body effect.
In your dc calculations, also assume $\lambda = 0$.

a) Specify the aspect ratios (W/L) of all transistors, such that:

- **All transistors operate at $|V_{OV}| = 0.25V$,**
  except input transistors Q_1 and Q_2 which operate at $V_{OV1} = V_{OV2} = 0.1$ V.
- **Input transistors Q_1 and Q_2 provide $g_{m1} = g_{m2} = 2$ mA/V.**

Note: do not assume that transistors Q_3 and Q_4 have the same (W/L).

$$g_{m1,2} = \mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} V_{OV1,2} = (200\mu A/V^2)\left(\frac{W}{L}\right)_{1,2}(0.1V) = 2mA/V \Rightarrow \left(\frac{W}{L}\right)_{1,2} = 100$$

Now, $I_{D1,2} = \frac{1}{2} g_{m1,2} \times V_{OV1,2} = 0.1mA$.

Hence, $I_{D5,6} = I_{D1,2} = 0.1mA$ and $I_{D3} = I_{D1} + I_{D2} = 0.2mA$.

Therefore, $$(W/L)_{5,6} = \frac{2\,I_{D5,6}}{\mu_p C_{ox} V_{OV5,6}^2} = \frac{2(0.1mA)}{(50\mu A/V^2)(0.25V)^2} = 64$$

$$(W/L)_3 = \frac{2\,I_{D3}}{\mu_n C_{ox} V_{OV3}^2} = \frac{2(0.2mA)}{(200\mu A/V^2)(0.250V)^2} = 32$$

$$(W/L)_4 = \frac{2\,I_{REF}}{\mu_n C_{ox} V_{OV3}^2} = \frac{2(25\mu A)}{(200\mu A/V^2)(0.25V)^2} = 4$$

b) Write the expression for the output resistance R_o. Find its value.

$$r_{o2} = \frac{1}{\lambda_n I_{D2}} = \frac{1}{(0.25V^{-1})(0.1mA)} = 40\ \text{k}\Omega$$

$$r_{o6} = \frac{1}{\lambda_p I_{D2}} = \frac{1}{(0.4V^{-1})(0.1mA)} = 25\ \text{k}\Omega$$

$$\therefore\ R_o = r_{o2} \| r_{o6} = 15.4\ k\Omega$$

c) Write the expression for the differential voltage gain $A_d = v_o/v_{id}$. Find its value.

The small-signal current through $Q1$ and $Q2$ in Fig. 1 is:

$$i_d = \frac{v_{id}}{2(1/g_{m1,2})} = g_{m1,2}\frac{v_{id}}{2}$$

and, therefore,

$$v_o = (2i_d)R_o = (g_m v_{id})R_o$$

where the factor 2 is due to the active load ($Q5$-$Q6$) which mirrors the current i_d, thereby doubling the total current at the output. Hence,

$$A_d = \frac{v_o}{v_{id}} = g_{m1,2}R_o = (2\text{mA/V})(15.4\text{k}\Omega) = 30.8\text{V/V}$$

d) To improve the gain of the CMOS amplifier in Fig. 1, the simple MOS current mirror (Q_5 - Q_6) can be replaced by a cascode MOS current mirror (Q_5 - Q_8), as shown in Fig. 2. Assuming $R_{o6} = \infty$, by what factor is the small-signal differential voltage gain A_d improved in Fig. 2, compared to Fig. 1? State why.

Assuming $R_{o6} = \infty$, the output resistance of the CMOS amplifier in Fig. 2 is:

$$R_o = r_{o2} \| R_{o6} \cong r_{o2} = 40\ \text{k}\Omega$$

Therefore, compared to Fig. 1, the small-signal differential voltage gain A_d in Fig, 2 is improved by a factor of:

$$\frac{A_d \text{ in Fig. 2}}{A_d \text{ in Fig. 1}} = \frac{R_o \text{ in Fig. 2}}{R_o \text{ in Fig. 1}} \cong \frac{r_{o2}}{r_{o2} \| r_{o6}} = \frac{40\ \text{k}\Omega}{15.4\ \text{k}\Omega} = 2.6$$

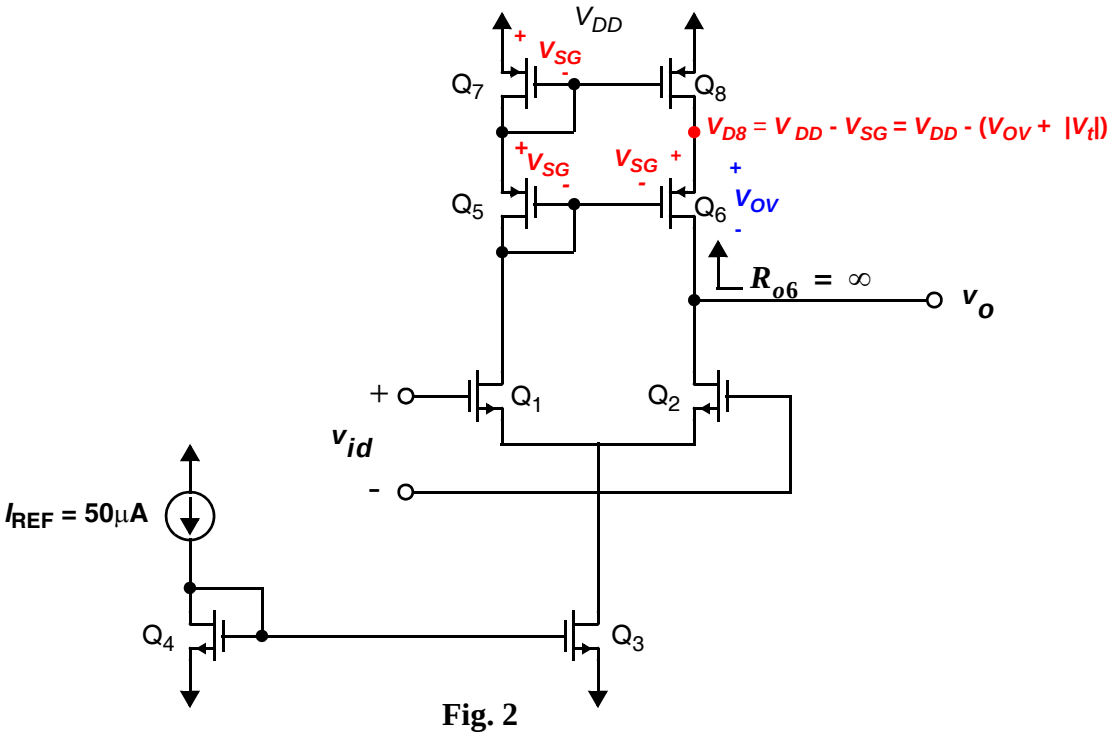

Fig. 2

e) Write expressions for the maximum output voltage $V_{o,\max}$ of the differential amplifiers in Figures 1 and 2. Here, $V_{o,\max}$ denotes the largest value of output voltage V_o for proper operation of the current mirror (Q_5-Q_6 in Fig. 1 and Q_5-Q_8 in Fig. 2), such that all its transistors are in saturation. Find their values, assuming transistors Q_5 - Q_8 operate at $|V_{OV}| = 0.25\text{V}$ and $V_{DD} = 2.5\text{V}$.

Since all PMOS transistors have the same overdrive voltage, let

$$V_{GS} \equiv V_{GS5} = V_{GS6} = V_{GS7} = V_{GS8} = V_{OV} + |V_{tp}| = 0.25\text{V} + 0.65\text{V} = 0.9\text{V}$$

In Figure 1, for Q_6 to remain in saturation:

$$V_{SD8} = V_{DD} - V_o \geq V_{OV} \Rightarrow V_{o,\max} = V_{DD} - V_{OV} = 2.5\text{V} - 0.25\text{V} = 2.25\text{V}$$

In Figure 2 (see circuit schematic):

$$V_{D8} = V_{DD} - V_{GS} = V_{DD} - (V_{OV} + |V_{tp}|)$$

Therefore, for Q_6 to remain in saturation:

$$V_{SD8} = V_{D8} - V_o \geq V_{OV} \Rightarrow V_{o,\max} = V_{DD} - (2V_{OV} + |V_{tp}|) = 1.35\text{V}$$

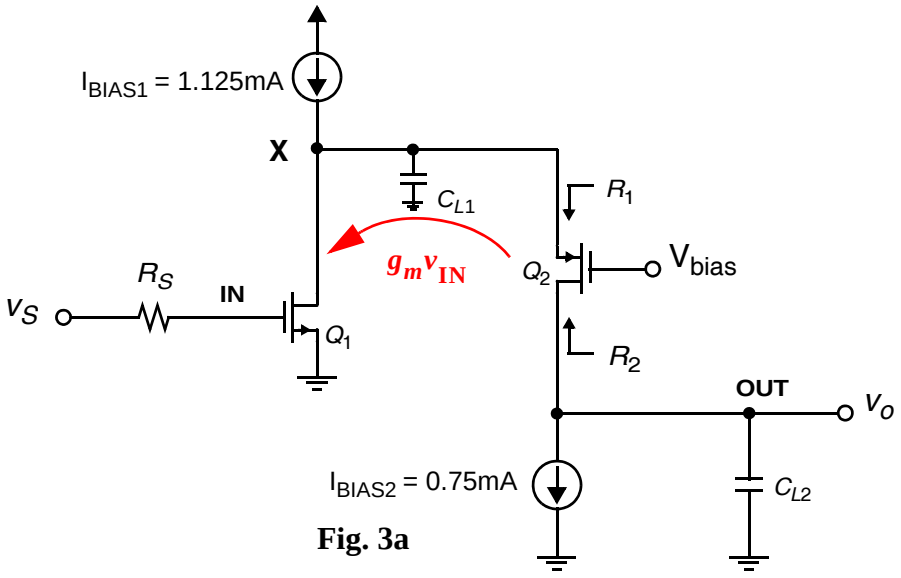

Fig. 3a

Question 2: [30 marks]

Consider the folded-cascode amplifier in Fig. 3. Assume that:

- **All MOSFETs are biased in the saturation region with $|V_{OV}| = 0.1\text{V}$.**
- **All NMOS and PMOS devices have their substrate (body) connected to ground and V_{DD}, respectively.**
- **$\gamma = 0$ and $\lambda = 0$, in your dc calculations.**
- **$g_{mb} = 0$, in your small-signal analysis.**
- **Current sources I_{BIAS1} and I_{BIAS2} have incremental output resistances of R_{L1} and R_{L2}, respectively.**
- **Capacitances C_{L1} and C_{L2} model the parasitic capacitances at nodes *X* and *OUT*, respectively, except for the parasitic (internal) capacitances of the MOSFETs.**
- **Do not neglect C_{db} in the MOSFET small-signal models.**

a) Find the value of transconductances g_{m1} and g_{m2} of transistors Q_1 and Q_2, respectively.

$I_{D1} = I_{BIAS1} - I_{BIAS2} = 0.375\text{mA} \Rightarrow g_{m1} = (2\,I_{D1})/V_{OV} = (2 \times 0.375\text{mA})/(0.1\text{V}) = 7.5\text{mA/V}$

$I_{D2} = I_{BIAS2} = 1\text{mA} \Rightarrow g_{m2} = (2\,I_{D2})/V_{OV} = (2 \times 0.75\text{mA})/(0.1\text{V}) = 15\text{mA/V}$

b) Write an expression for resistances R_1 and R_2 at midband frequencies.

$$R_1 \cong \frac{1}{g_{m2}}\left(1 + \frac{R_{L2}}{r_{o2}}\right)$$

$$R_2 \cong (R_{L1} \,\|\, r_{o1}) + r_{o2}[1 + g_{m2}(R_{L1} \,\|\, r_{o1})]$$

c) Write an expression of the midband voltage gains $A_{M1} \equiv v_x/v_{in}$ and $A_M \equiv v_o/v_s$.

$v_{\text{in}} = v_s$

$i_d = g_{m1} v_{\text{in}}$ (see circuit diagram in Fig. 3a)

$v_x = i_d(r_{o1} \,\|\, R_{L1} \,\|\, R_1) \Rightarrow A_{M1} = v_x/v_{in} = -g_{m1}(r_{o1} \,\|\, R_{L1} \,\|\, R_1)$

$v_o = i_d(R_{L2} \,\|\, R_2) \Rightarrow A_M = v_o/v_s = -g_{m1}(R_{L2} \,\|\, R_2)$

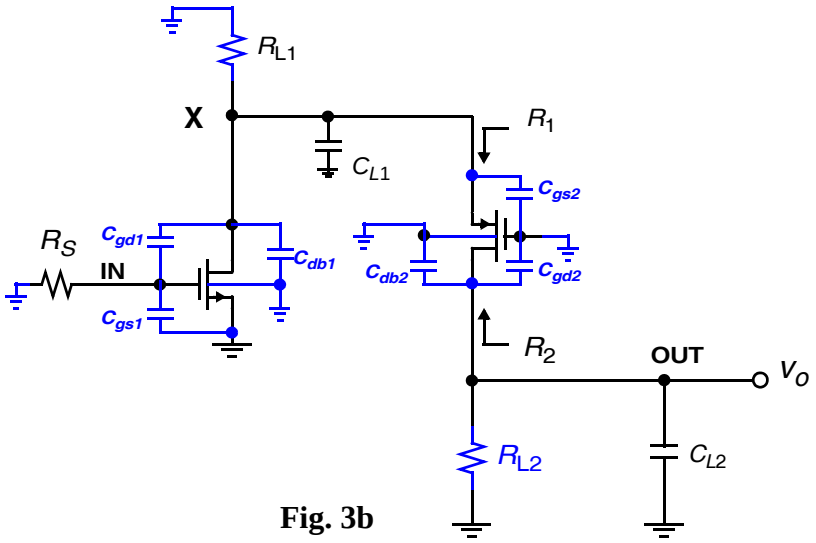

Fig. 3b

d) Write an expression for the high-frequency poles associated with nodes *IN*, *X*, and *OUT*.

Hint: Apply Miller's theorem, then find the open-circuit time constants.

Note: For simplicity, write your expressions using the previously-derived variables, together with the MOSFET small-signal parameters.

The above circuit diagram (Fig. 3b) can be used to determine the high-frequency poles of the amplifier.

Node IN:

Using Miller theorem, C_{gd1} is replaced by $C_{gd1}(1 + |A_{M1}|)$ between node IN and GND.

The total capacitance associated with node IN is then: $C_{IN} = C_{gs1} + C_{gd1}(1 + |A_{M1}|)$

The total resistance associated with C_{IN} is: $R_{IN} = R_S$

The open-circuit time constant associated with C_{IN} is: $\tau_{IN} = R_{IN}C_{IN}$

The pole associated with node IN is: $\omega_{IN} = 1/\tau_{IN}$

Node X:

Using Miller theorem, C_{gd1} is replaced by $C_{gd1}(1 + 1/|A_{M1}|)$ between node X and GND.

The total capacitance associated with node X is then: $C_X = C_{gd1}(1 + 1/|A_{M1}|) + C_{db1} + C_{L1} + C_{gs2}$

The total resistance associated with C_X is: $R_X = r_{o1} \parallel R_{L1} \parallel R_1$

The open-circuit time constant associated with C_X is: $\tau_X = R_X C_X$

The pole associated with node *X* is: $\omega_X = 1/\tau_X$

Node OUT:

The total capacitance associated with node X is then: $C_{OUT} = C_{gd2} + C_{db2} + C_{L2}$

The total resistance associated with C_{OUT} is: $R_{OUT} = R_{L2} \parallel R_2$

The open-circuit time constant associated with C_{OUT} is: $\tau_{OUT} = R_{OUT}C_{OUT}$

The pole associated with node OUT is: $\omega_{OUT} = 1/\tau_{OUT}$

e) Assuming a dominant pole exists, estimate:

i) the 3-dB frequency, based on the open-circuit time-constant approximation

$$\omega_{3dB} \cong 1/(\tau_{IN} + \tau_X + \tau_{OUT})$$

ii) the unity-gain frequency

Note: For simplicity, write your expressions using the previously-derived variables.

$$\omega_t \cong A_M \omega_{3dB}$$

f) Current sources I_{BIAS1} and I_{BIAS2} in Fig. 3 can be realized using, respectively, current sources $Q3$-$Q4$ and $Q5$-$Q6$, as shown in Fig. 4.
Assume that the signal voltage at the gate of $Q3$ and $Q5$ in Fig. 4 is zero.

For the expressions found in parts (b)-(d) for the circuit in Fig. 3, which variables must be replaced and by which variables in Fig. 4 must they be replaced, in order to obtain the corresponding expressions for the circuit in Fig. 4 ?

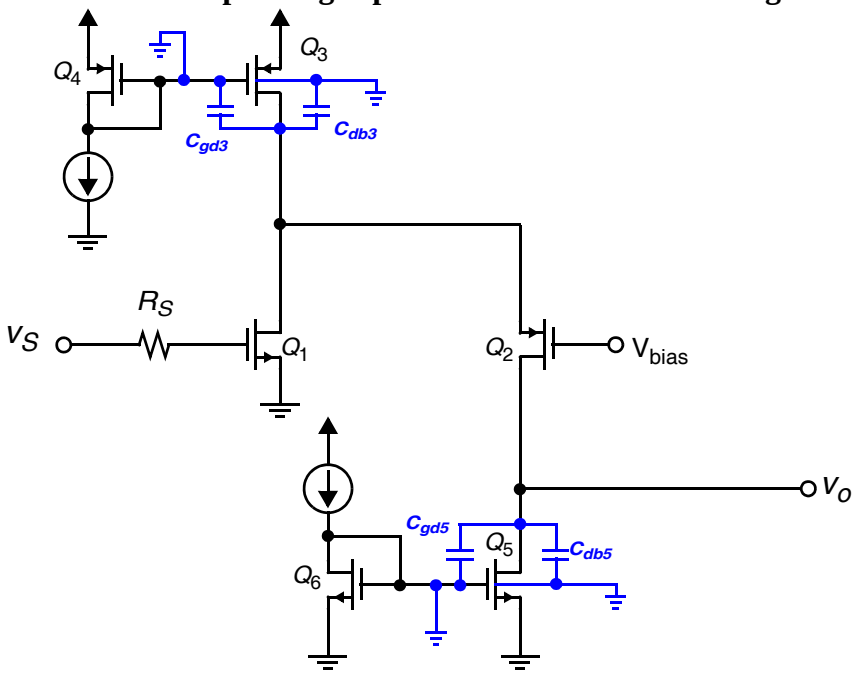

Fig. 4

Exchange:

- R_{L1} with r_{o3} (to account for the output resistance of current source I_{BIAS1})
- R_{L2} with r_{o5} (to account for the output resistance of current source I_{BIAS2})
- C_{L1} with $C_{gd3} + C_{db3}$ (to account for the effect of the internal capacitance of Q3 on the total capacitance at node X).
- C_{L2} with $C_{gd5} + C_{db5}$ (to account for the effect of the internal capacitance of Q5 on the total capacitance at node OUT).