McGill University

Faculty of Engineering
Department of Electrical and Computer Engineering
ECSE-330A – Introduction to Electronics

Examiner: Dr. David V. Plant; _____________________
Associate Examiner: Dr. Ramesh Abhari ______________________
Date: Monday, December 12, 2005
Time: 2:00 – 5:00
Calculator: Faculty Standard

Pertinent Information:

1) This is a closed-book examination, no notes permitted. There are 3 pages of equations provided at the back of the examination.

2) The examination consists of 6 problems; you must answer all 6 problems.

3) The examination is worth 66 total points

4) The examination consists of 10 pages, including this page and the equations pages; please ensure you have a COMPLETE examination paper.

5) Only the Faculty Standard Calculator is permitted.

6) Questions may be completed in any order, however ensure that you clearly identify which part of which question you are attempting.

Do NOT turn in this exam with your exam booklet

Question #1 (12 pts.):

Two amplifiers are cascaded to provide current to drive the load as shown in Fig 1a.

A_1 is a **voltage amplifier** and A_2 is a **transconductance amplifier**.

Both A_1 and A_2 have **Rin = Rout = R**.

Assume all the diodes are identical and use the constant-voltage drop model.

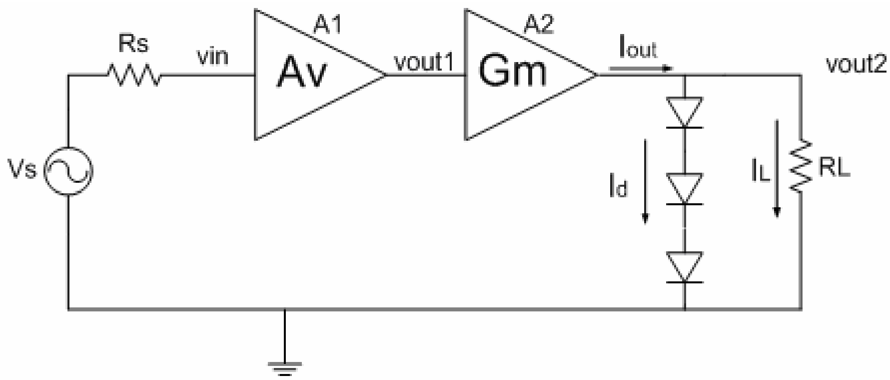


Fig. 1a

a) [3 pts.] Redraw the circuit and replace the amplifiers with their equivalent circuits. (Note: Leave the diodes as they are, do not replace them with a small signal model).

b) [3 pts.] Assuming all the diodes are OFF, find an expression for the overall transconductance $G_{m\_tot} = I_{out}/v_s$ in terms of the R_s, R, R_L, A_v and G_m.

For part c), use $R_s = 1k\Omega$, $R_{in} = R_{out} = 10k\Omega$, $R_L = 2k\Omega$, $A_v = 200V/V$, $Gm = 500mA/V$.

c) [3 pts.] If the current flow through the diodes is $I_d = 5mA$, calculate v_s.

d) [3 pts.] For the circuit shown in Fig 1b, find an expression for the voltage gain v_{out}/v_s. Do NOT simplify your answer. (Hint: using KCL.)

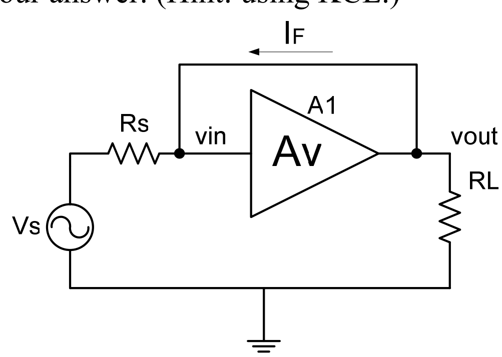


Fig 1b

Question #2 (12 pts.):

Consider the following circuit (Fig 2). Use the constant-voltage-drop model for the diodes. The pnp BJT is in the active mode and has $|V_{BE}| = 0.7$ and $\beta=49$. All capacitors are infinite and all diodes have n=2.

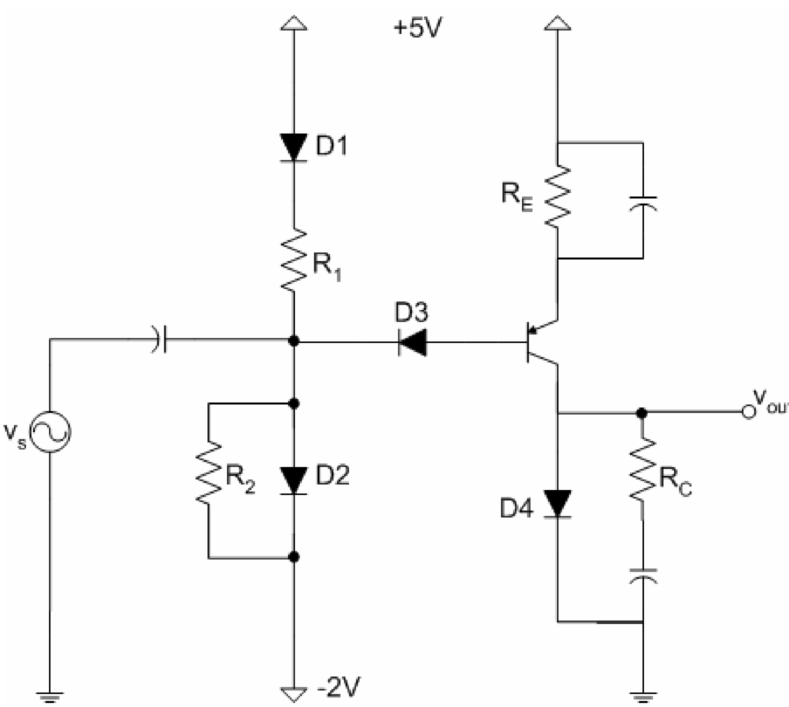


Fig 2.

You may use the following values:
R_1 = 11.2 kΩ **R_2 = 3.5 kΩ**
R_E = 980 Ω **R_C = 100 Ω**

You may neglect the Early Effect for all parts of this question.

a) [4 pts.] Determine which diodes (D1-D4) are on or off, and calculate the currents (I_{D1}-I_{D4}) through each diode. *State your assumptions clearly.*

b) [1 pt] What is the minimum R_2 so that diode D2 is on?

c) [3 pts] Draw the small-signal equivalent circuit, calculating the values of the small-signal parameters involved (use your currents from part **a)**). You may neglect the Early effect.

d) [2 pts.] Calculate the voltage gain $v_{out}/v_{s.}$

e) [2 pts] If a resistive load were attached to the output node (without affected the DC operating point), would the gain in part **d)** increase or decrease? Why?

Question #3 (11 pts):

The following circuit (Fig 3) is a MOSFET differential pair with active loads. All FETs are in saturation mode. Note that M3 is diode-connected and M4 is not. Neglect channel-length modulation and the Body Effect for all transistors.

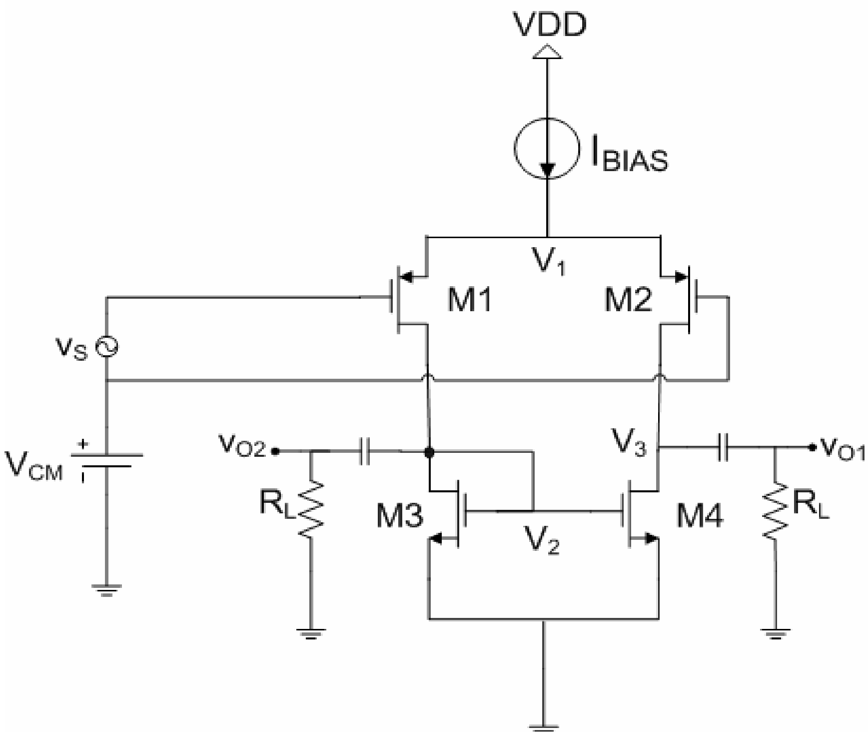


Fig. 3

You may use the following values:

$k_n' = 2*k_p' = 500\mu A/V^2$	$Vt_n = \|Vt_p\| = 0.7V$	$V_{DD} = 5V$
$W_1/L_1 = W_2/L_2 = 12.5$	$I_{BIAS} = 2mA$	$V_{CM} = 3V$
$W_3/L_3 = W_4/L_4 = 4$	$R_L = 5k\Omega$	

a) [3 pts] Find the value of the DC voltages V_1 and V_2. (Hint: There is still **DC symmetry** in this problem)

b) [1 pts] Find the upper and lower boundaries on the voltage V3 that will keep M1 and M4 in the saturation mode of operation

c) [2 pts] Draw the small-signal diagram for this circuit. (Hint: use T-models and replace M3 with an appropriate resistor. Recall: T-models have 0 gate current!)

d) [1 pt] Find the value for the small-signal parameters g_{m1}, g_{m2}, g_{m3}, and g_{m4}.

e) [2 pts.] Derive an expression for the gain v_{O2}/v_S and compute its value.

f) [2 pts] Derive an expression for the gain v_{O1}/v_S and compute its value.

Question #4 (10 pts.):

Consider the case of two inverters in series, as shown in Fig 4. You may assume that the P and N transistors are matched in each inverter.

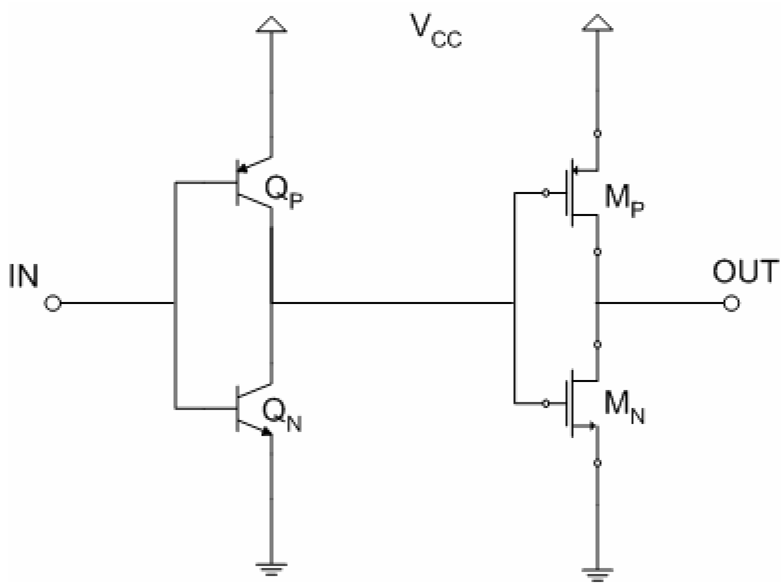


Fig. 4

You may use the following values:
V_{CC} = 5V
$|V_{CE\_SAT}|$ = 0.2V for all BJTs
$|V_t|$ = 1V for all FETs.

a) [2 pts] Describe the mode of operation (cut-off, triode, saturation or active) of the four transistors (Q_P, Q_N, M_P, M_N) when the input is 0V.

b) [1 pt] Sketch what the voltage transfer characteristic of this device will look like for inputs between 0V and 5V (you do not need to calculate V_{IL} and V_{IH}).

For parts c), d) and e) you must include the Early Effect and CLM

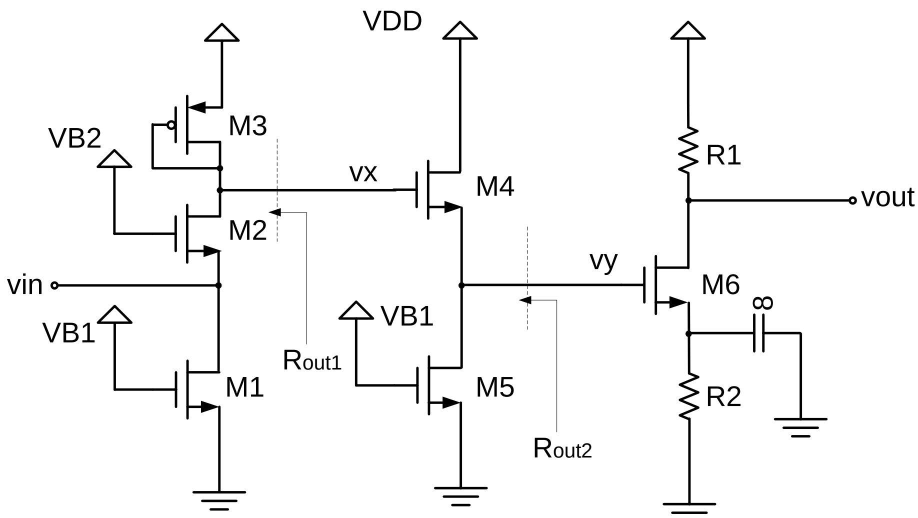
c) [3 pts] Draw a small-signal model for this circuit assuming all BJT's are active and all FETs are in saturation. (Do not calculate any values)

d) [2 pts] Assuming a small-signal voltage v_{in} at "IN", show that the overall gain v_{out}/v_{in} is $g_{mQ} \cdot r_{oQ} \cdot g_{mM} \cdot r_{oM}$ where 'Q' and 'M' denote BJTs and FETs, respectively.

e) [2 pts] The gain expression found in part **d)** does **NOT** depend on the DC biasing conditions of the BJTs (as long as they are active), but **DOES** depend on the DC biasing around the FETs. Explain why this is so. (Hint: check the formula sheets for clues).

Question 5 (10 pts.):

Consider the following circuit. All FETs are operating in saturation. You must decide for each FET whether or not to include Channel Length Modulation and the Body Effect in your analysis.



a) [1 pt.] This is a 3-stage amplifier. Identify the topology of each stage as common-gate (CGA), common-source (CSA) or common-drain (CDA).

b) [3 pts.] Draw the small signal equivalent circuit.

c) [1 pt.] Find an expression for v_x/v_{in}.

d) [1 pt.] Find an expression for v_y/v_x.

e) [1 pt.] Find an expression for v_{out}/v_y.

f) [1 pt.] Find an expression for R_{out1}.

g) [2 pt.] Find an expression for R_{out2}.

Question #6 (11 pts):

Consider the Bipolar-MOSFET circuit shown in Fig. 6. Use the rules established in class to determine if you must include channel-length modulation and the Early Effect. Neglect the body effect for all transistors. Assume the constant voltage drop model for all BJTs ($|V_{be}| = 0.7$) and a threshold voltage $|V_t| = 0.6$V for all FETs.

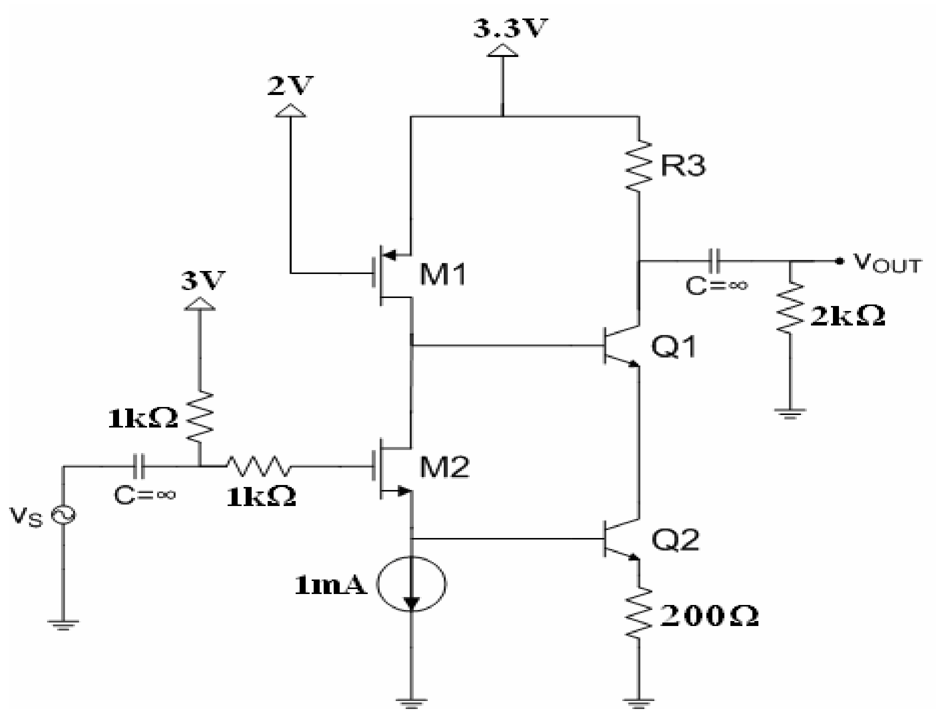


Fig. 6

You may use the following values:

$W_2/L_2 = 1$ **$\lambda = 0.05V^{-1}$** **$K_n' = 2{*}K_p' = 1mA/V^2$**

$\beta = \infty$ **$V_A = 60V$** **$V_{CE\text{-}SAT} = 0.2V$**

a) [2 pts] Find W_1/L_1 so that M1 is at the edge of triode and saturation operation.

b) [1 pt] With respect to the value found in a), would increasing W_1/L_1 put M1 in the triode or saturation mode of operation?

c) [3 pts] Find the value of R_3 that will result in a maximally symmetric voltage swing at the collector of Q1. (Hint: Solve V_{GS2} first)

For parts d) and e), do not solve for the small-signal parameters or calculate your answer. Include the output resistance of the current-source I_{BIAS}.

d) [2 pts] Draw the small-signal model for the circuit of Fig. 6. (Hint: Remember that $\beta = \infty$ for those BJT's, so $I_B = 0$)

e) [3 pts] Express the voltage gain v_{out}/v_s.

FORMULA SHEETS

Diodes:

$$i = I_S \exp(v / nV_T - 1)$$

$$r_d = nV_t / I_D$$

BJTs:

$$i_C = I_S \exp(v_{BE}/V_T)$$

$$i_B = \frac{i_C}{\beta}$$

$$i_E = \frac{i_C}{\alpha}$$

$$i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_E = (\beta+1) i_B$$

$$g_m = \frac{I_C}{V_T} \quad r_e = \frac{V_T}{I_E} = \alpha \frac{V_T}{I_C} = \frac{\alpha}{g_m}$$

$$r_\pi = \frac{V_T}{I_B} = \frac{\beta}{g_m} \quad r_o = \frac{V_A}{I_C}$$

$$r_\pi = (\beta+1) r_e$$

$$\beta = \frac{\alpha}{1-\alpha} \quad \alpha = \frac{\beta}{\beta+1} \quad \beta+1 = \frac{1}{1-\alpha}$$

FETs:

NMOS:

Cutoff: $V_{GS} < V_t$ $I_D = 0$

Triode: $V_{GS} > V_t$, $V_{DS} < V_{GS} - V_t$ $I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$

Saturation: $V_{GS} > V_t$, $V_{DS} > V_{GS} - V_t$ $I_D = \tfrac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

Body effect: $V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$

PMOS:

Cutoff: $V_{GS} > V_t$ $I_D = 0$

Triode: $V_{GS} < V_t$, $V_{DS} > V_{GS} - V_t$ $I_D = k_p' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$

Saturation: $V_{GS} < V_t$, $V_{DS} < V_{GS} - V_t$ $I_D = \tfrac{1}{2}k_p' \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

Body effect: $|V_t| = |V_{t0}| + \gamma\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$

SMALL SIGNAL

$$g_m = \frac{2 \cdot I_D}{V_{GS} - V_t}$$

$$g_m = k_n' \frac{W}{L}(V_{GS} - V_t)(1 + \lambda \cdot V_{DS})$$

$$g_m = \sqrt{2k_n'}\sqrt{\frac{W}{L}}\sqrt{1 + \lambda \cdot V_{DS}}\sqrt{I_D}$$

$$r_o = \frac{1}{\lambda \cdot I_D}$$

$$g_{mb} = \chi \cdot g_m$$

$$\chi = \frac{\gamma}{2} \cdot \frac{1}{\sqrt{2\phi_f + V_{SB}}}$$