Chapter 4

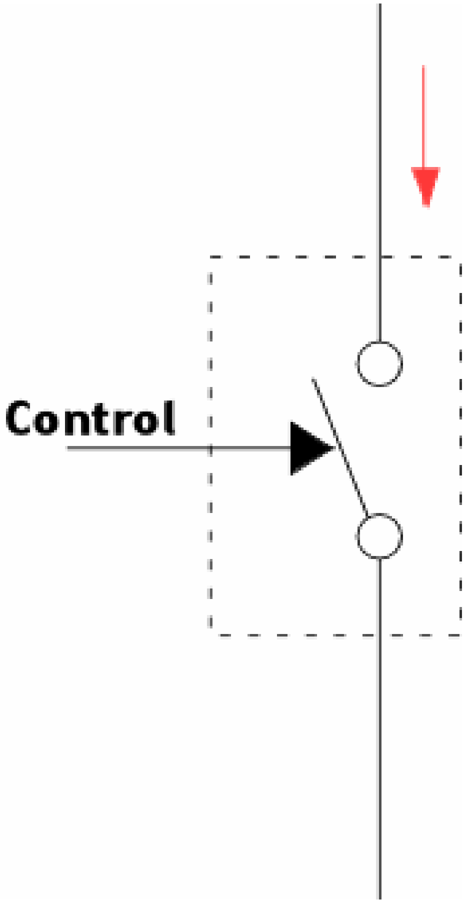
Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

Sedra/Smith, Sections 4.1- 4.10, {also 10.3, 6.3}

Outline of Chapter 4

- *1- Intro to MOS Field Effect Transistor (MOSFET)*
- 2- NMOS FET
- 3- PMOS FET
- 4- DC Analysis of MOSFET Circuits
- 5- MOSFET Amplifier
- 6- MOSFET Small Signal Model
- 7- MOSFET Integrated Circuits
- 8- CSA, CGA, CDA
- 9- CMOS Inverter & MOS Digital Logic

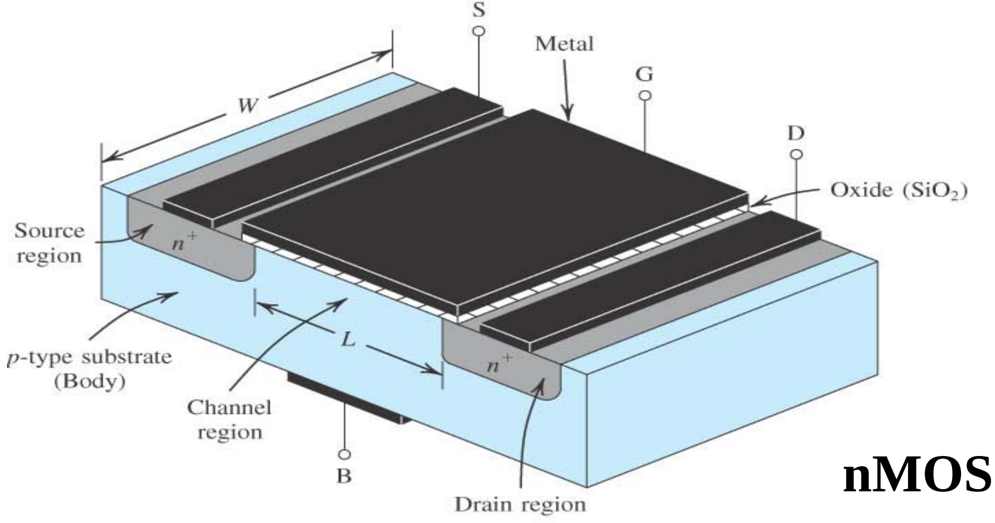
Transistors



- A ***three*** terminal device is required to implement current switches and amplifiers.
  - need voltage control terminal
  - used to control current flow through other two terminals
- All four ideal amplifier configurations (Chapter 1) employ dependent sources.
- A small control voltage can allow a large change in current.

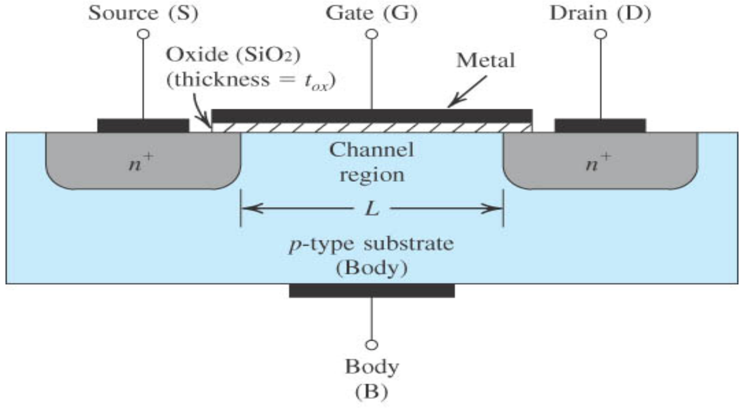
Transistors-Two PN Junctions

- Metal Oxide Semiconductor Field-Effect Transistors (MOSFET)



(a)

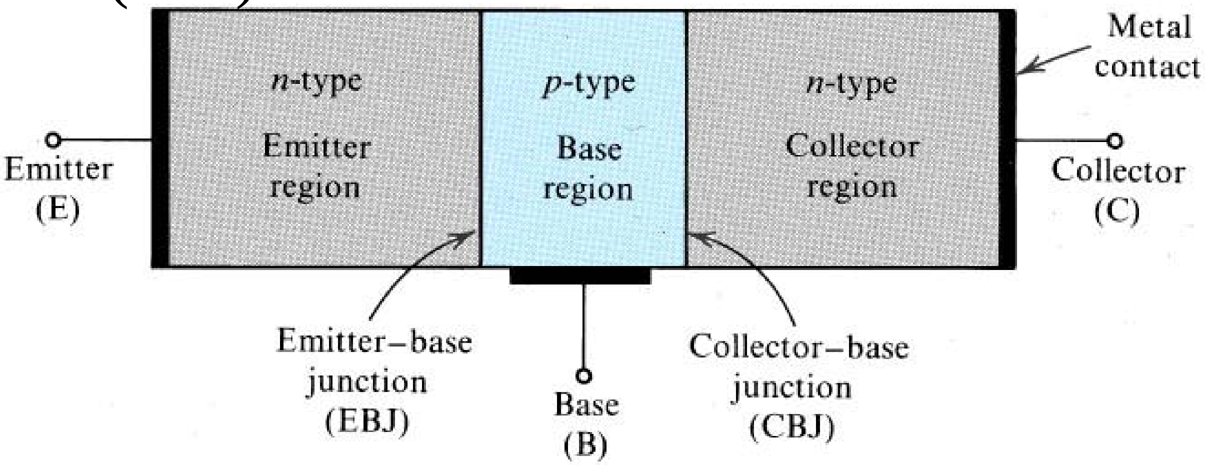
nMOS



(b)

- Bipolar Junction Transistor (BJT)

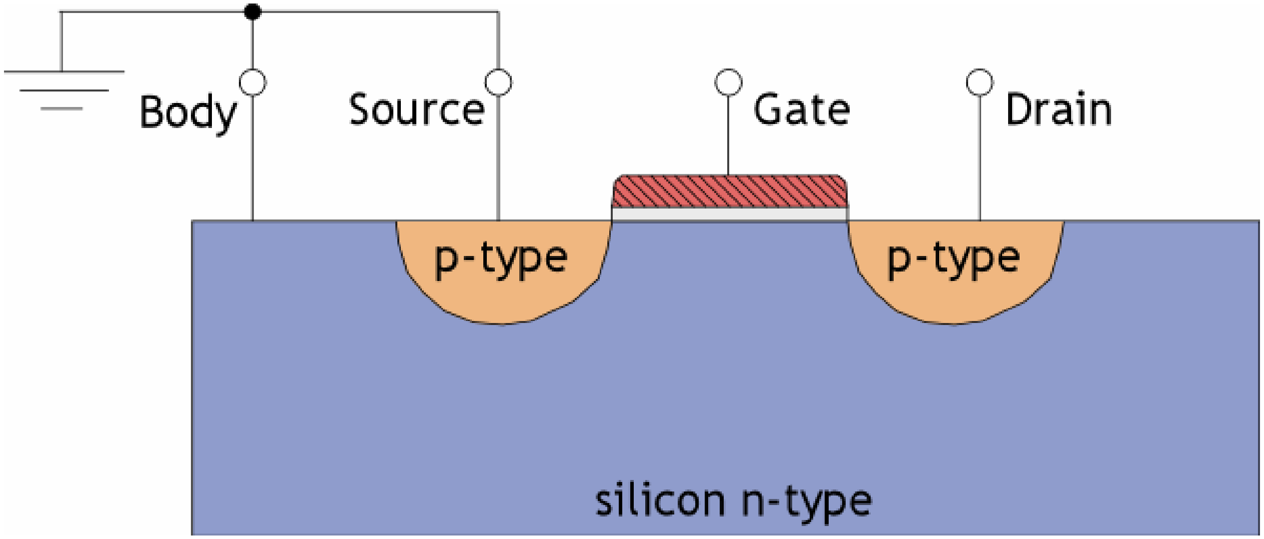
npn



Transistors-Two PN Junctions

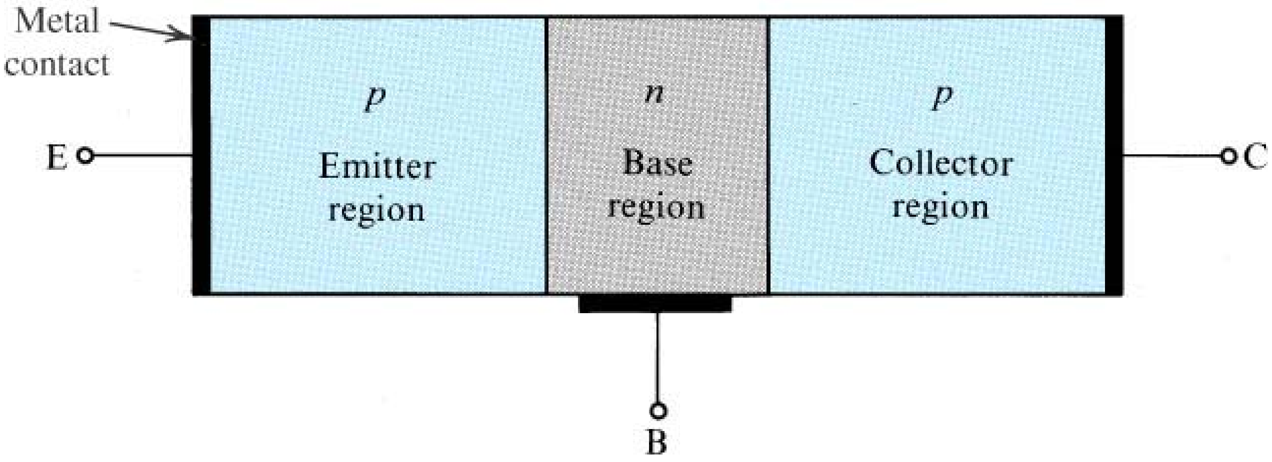
- Metal Oxide Semiconductor Field-Effect Transistors (MOSFET)

pMOS



- Bipolar Junction Transistor (BJT)

pnp

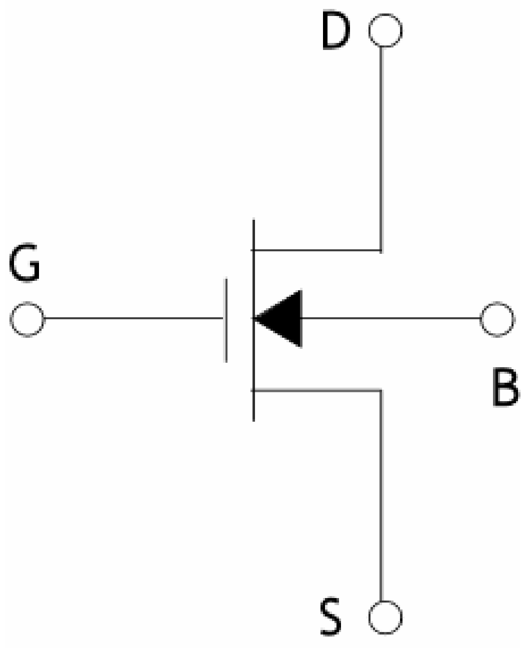


Basic Characteristics of the MOSFET

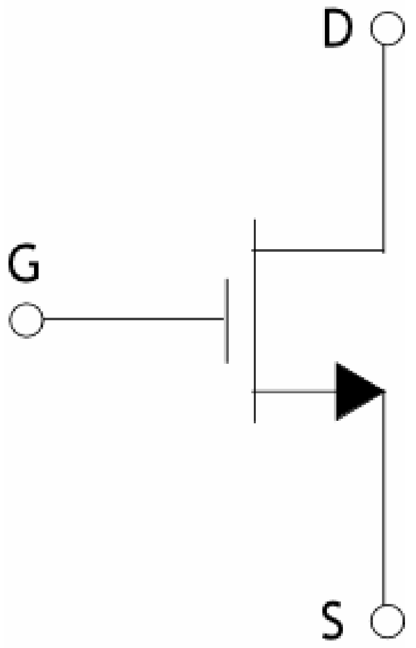
- The current flows parallel to the surface.
- The MOSFET is usually smaller than the BJT.
  - It consumes less power.
  - It has a much smaller transconductance, g_m, because of its small cross-sectional area.
- Massive integration techniques for digital applications.
- BJTs generally have better performance (predictable small signal parameters).
- Modern digital very-large-scale-integrated (VLSI) circuits employ MOSFETs almost exclusively.
- Analog applications use BJTs only when ***top*** performance is absolutely essential.

nMOS Circuit Symbol

- A MOSFET is a ***four-terminal*** device
- Body terminal is ***always*** biased at ***most negative*** potential

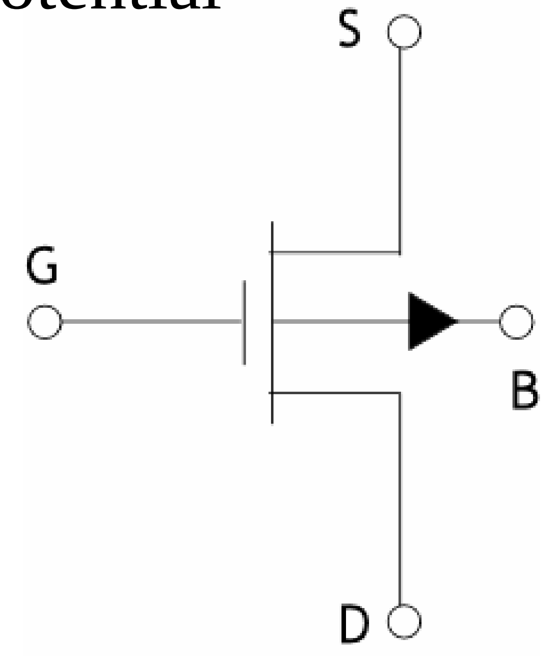


- Simplified symbol with implicit Body terminal connection
- Arrow indicates direction of current

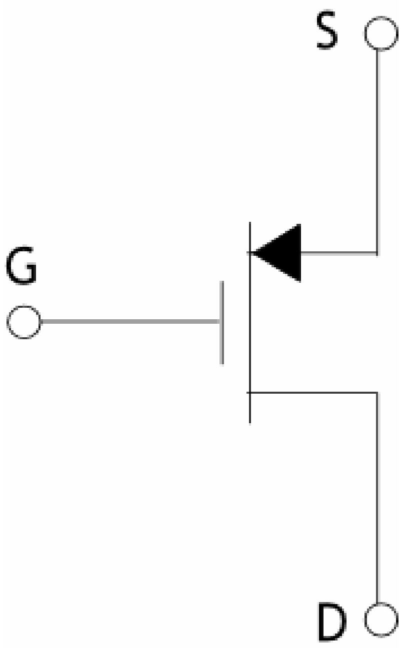


pMOS Circuit Symbol

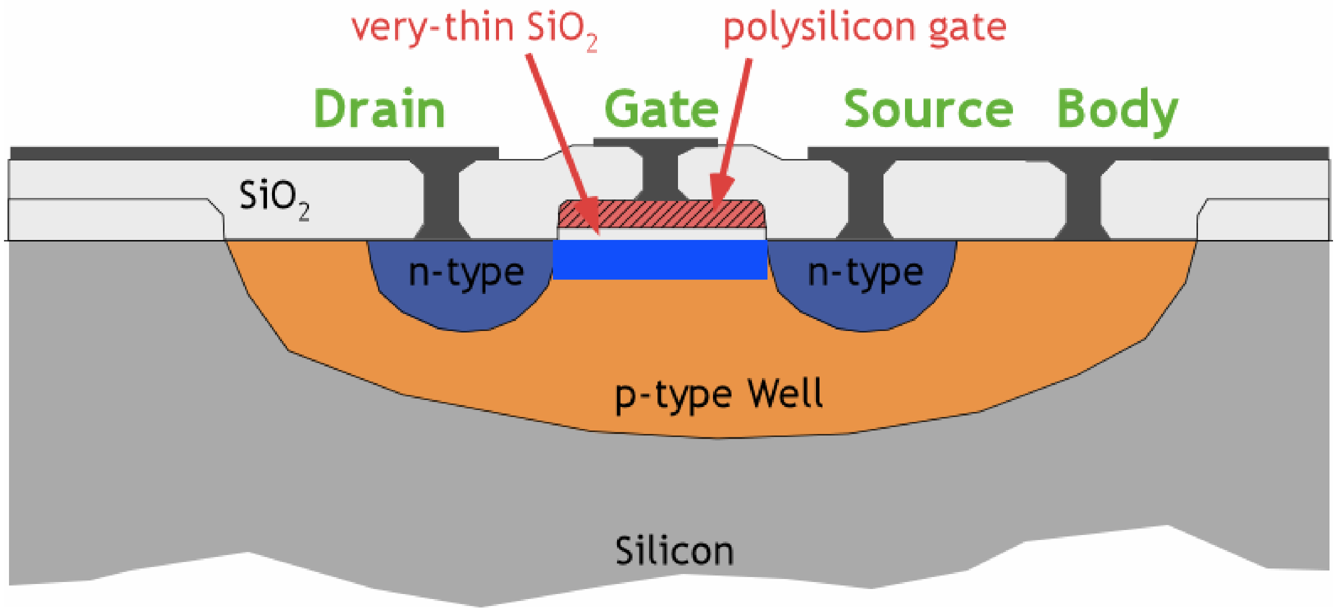
- A MOSFET is a ***four terminal*** device
- Body terminal is ***always*** biased at ***most positive*** potential



- Simplified symbol with implicit Body terminal connection
- Arrow indicates direction of current flow



The n-channel MOSFET (nMOS)

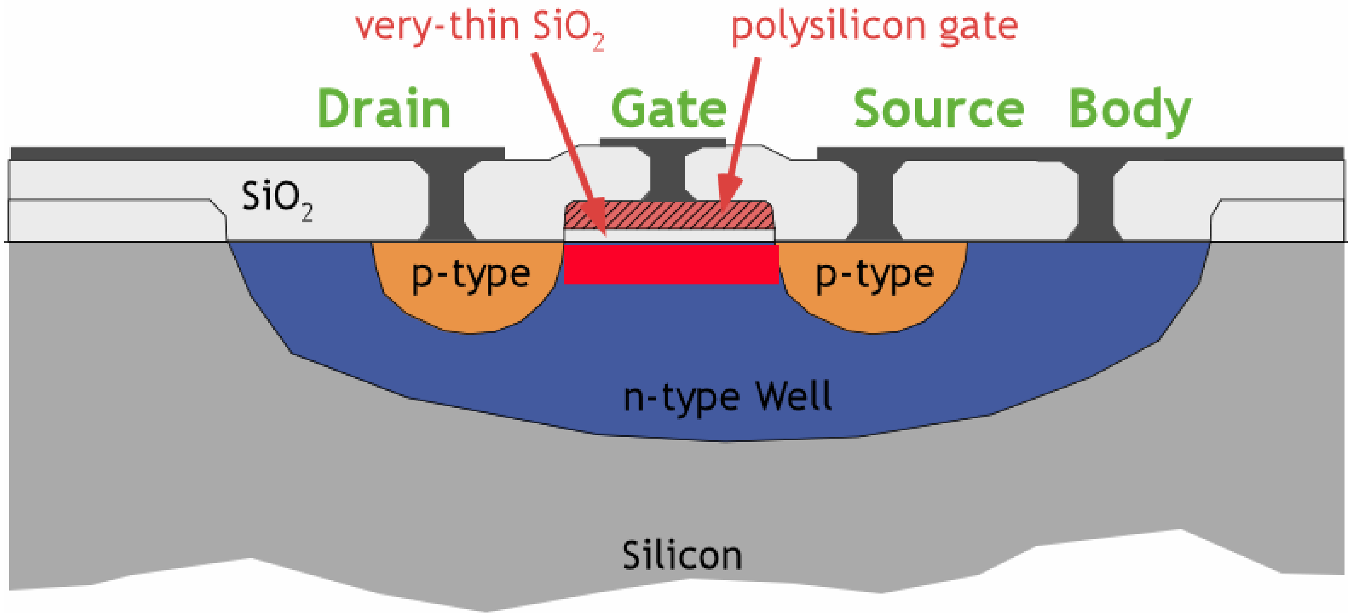


- nMOS created in p-type well, this is the Body
- Heavily doped n+ Drain and Source regions. Usually Body and Source connected.

- Gate electrode over thin SiO_2 dielectric forms parallel plate capacitor with Body

This defines the *n-channel*

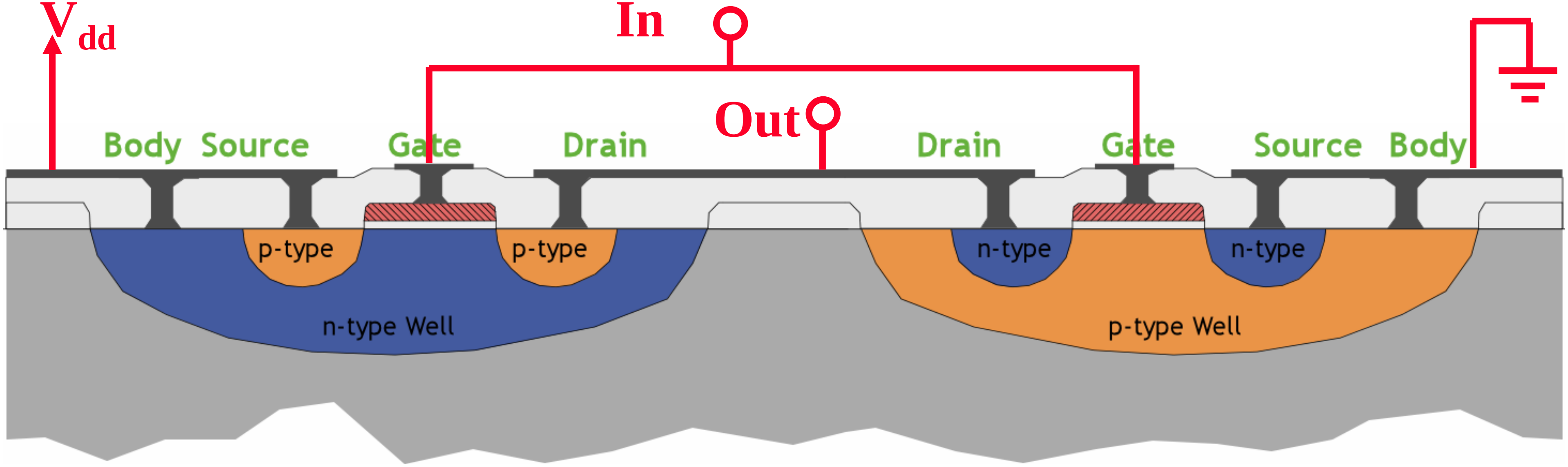
The p-channel MOSFET (pMOS)



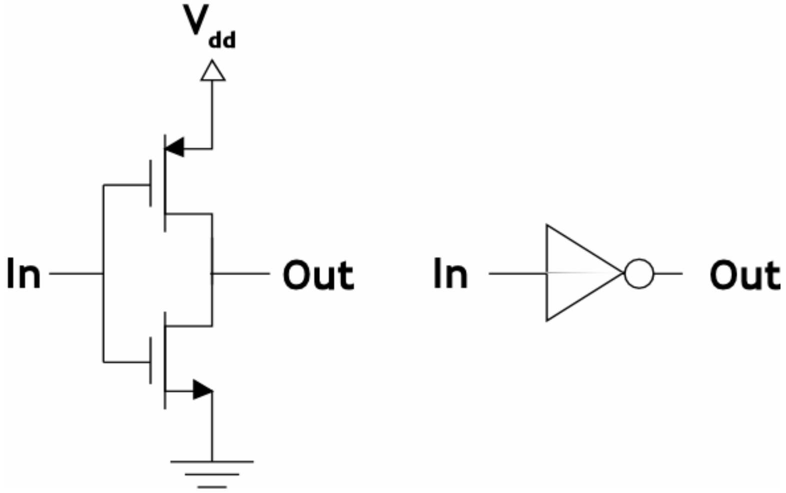
- pMOS created in n-type well, this is the Body
- Heavily doped p+ Drain and Source regions. Usually Body and Source connected.
- Gate electrode over thin SiO_2 dielectric forms parallel plate capacitor with Body

This defines the *p-channel*

Complementary MOS Technology (CMOS)



- CMOS technologies provide nMOS and pMOS devices
- The example shown called dual-well technology.
- p-well ***only*** and n-well ***only*** technologies also exist



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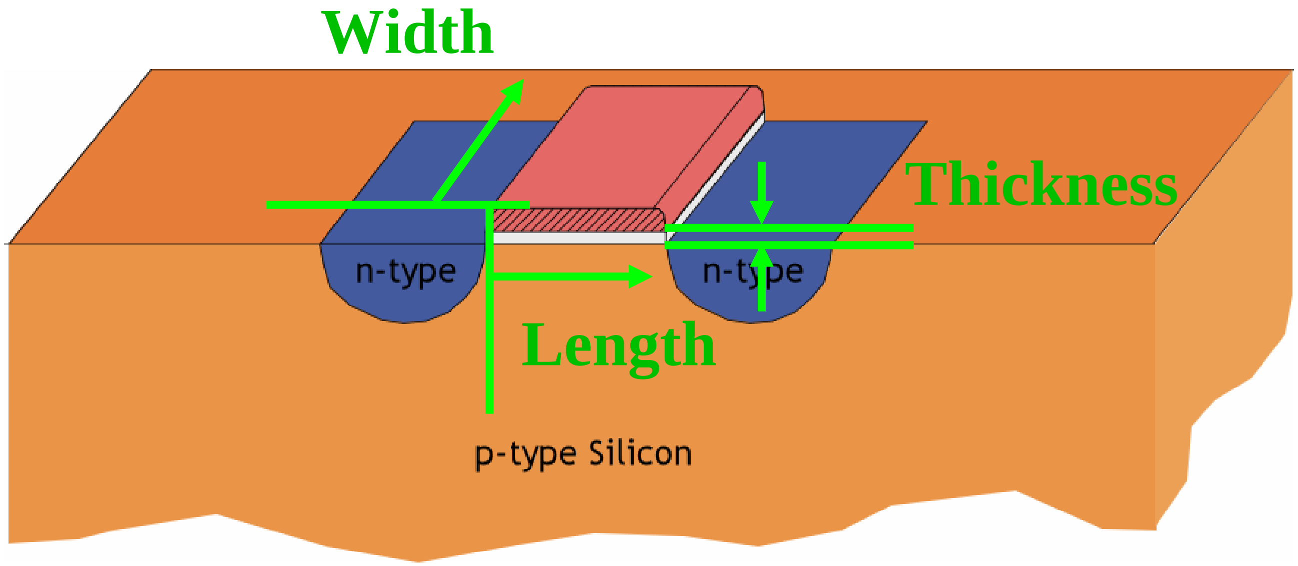
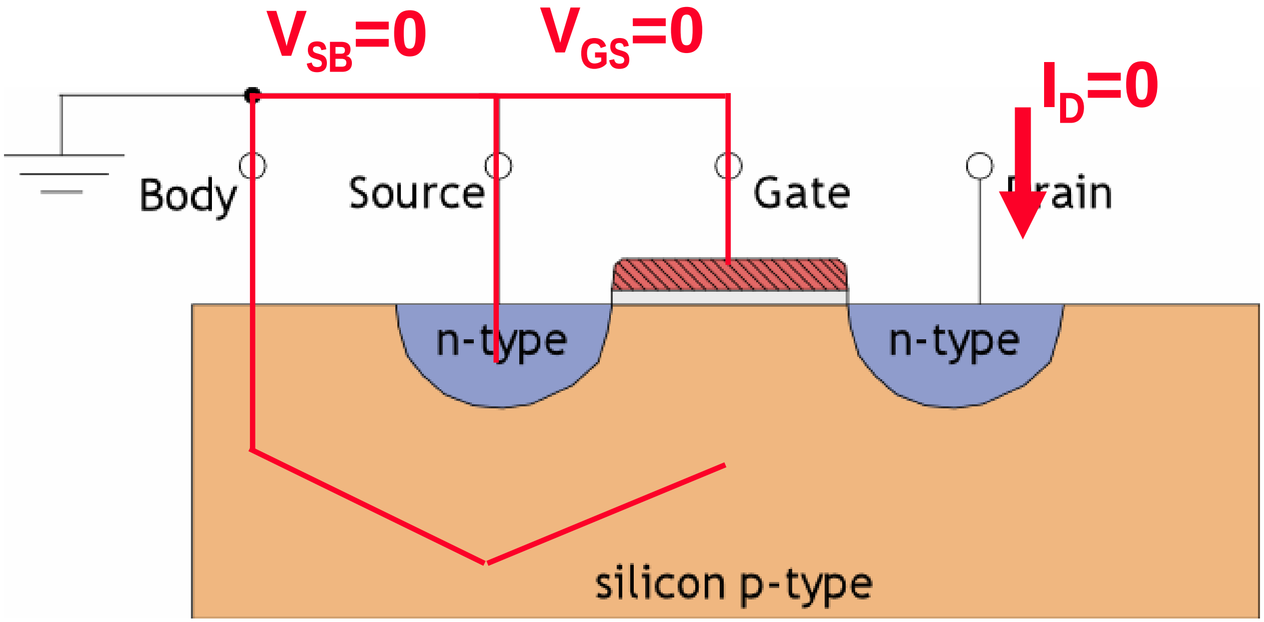
The n-Channel Enhancement MOSFET



- B-S & B-D pn junctions kept reverse-biased with the body terminal the most negative (or attached to the source).
- Aspect ratio of nMOS (W/L) chosen freely, affects g_m.

- Parameters
  - Channel Length (L)
  - Channel Width (W)
  - Oxide Thickness (t_{OX})
  - Oxide permittivity (ε_{OX})
  - Electron Mobility (μ_n)

nMOS Channel Cut-off



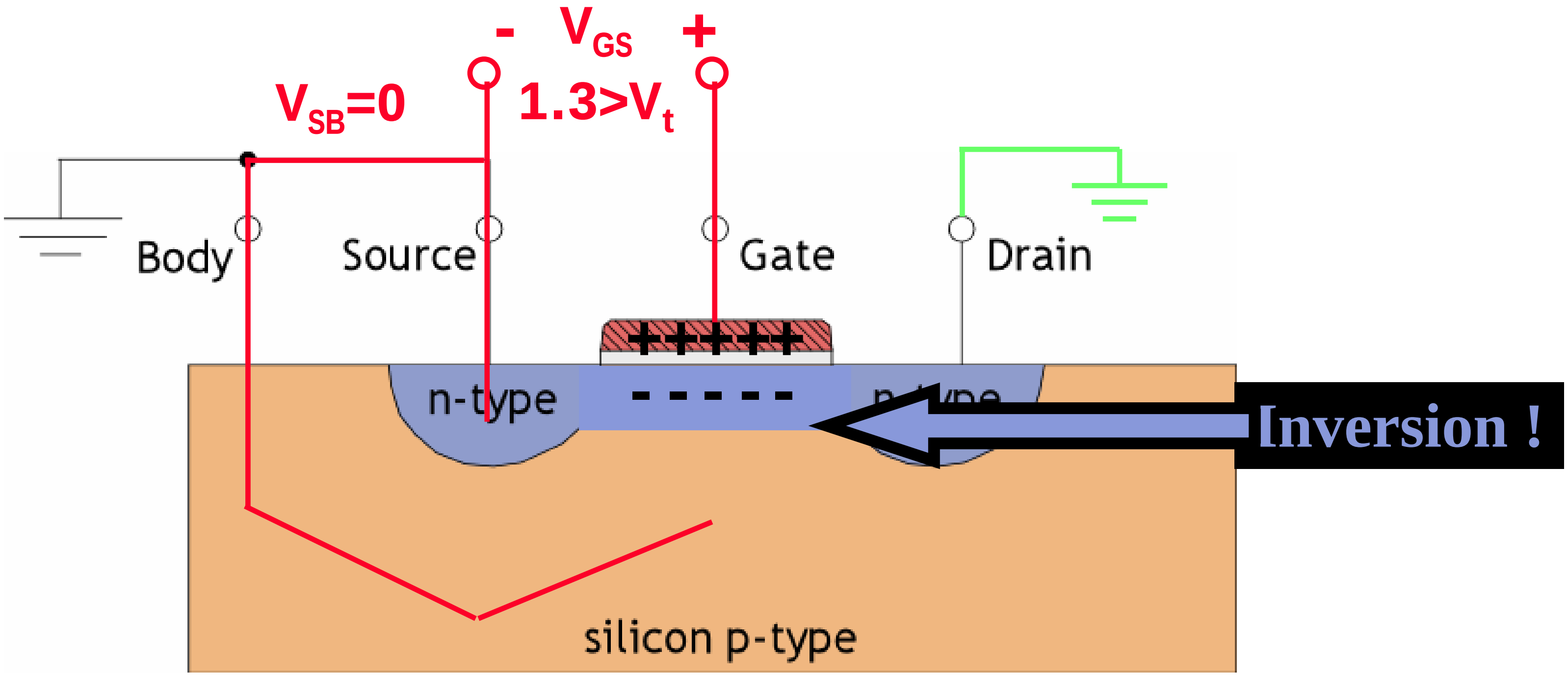
Cut-Off

$$\boxed{V_{GS} < V_t}$$

$$\boxed{I_D = 0}$$

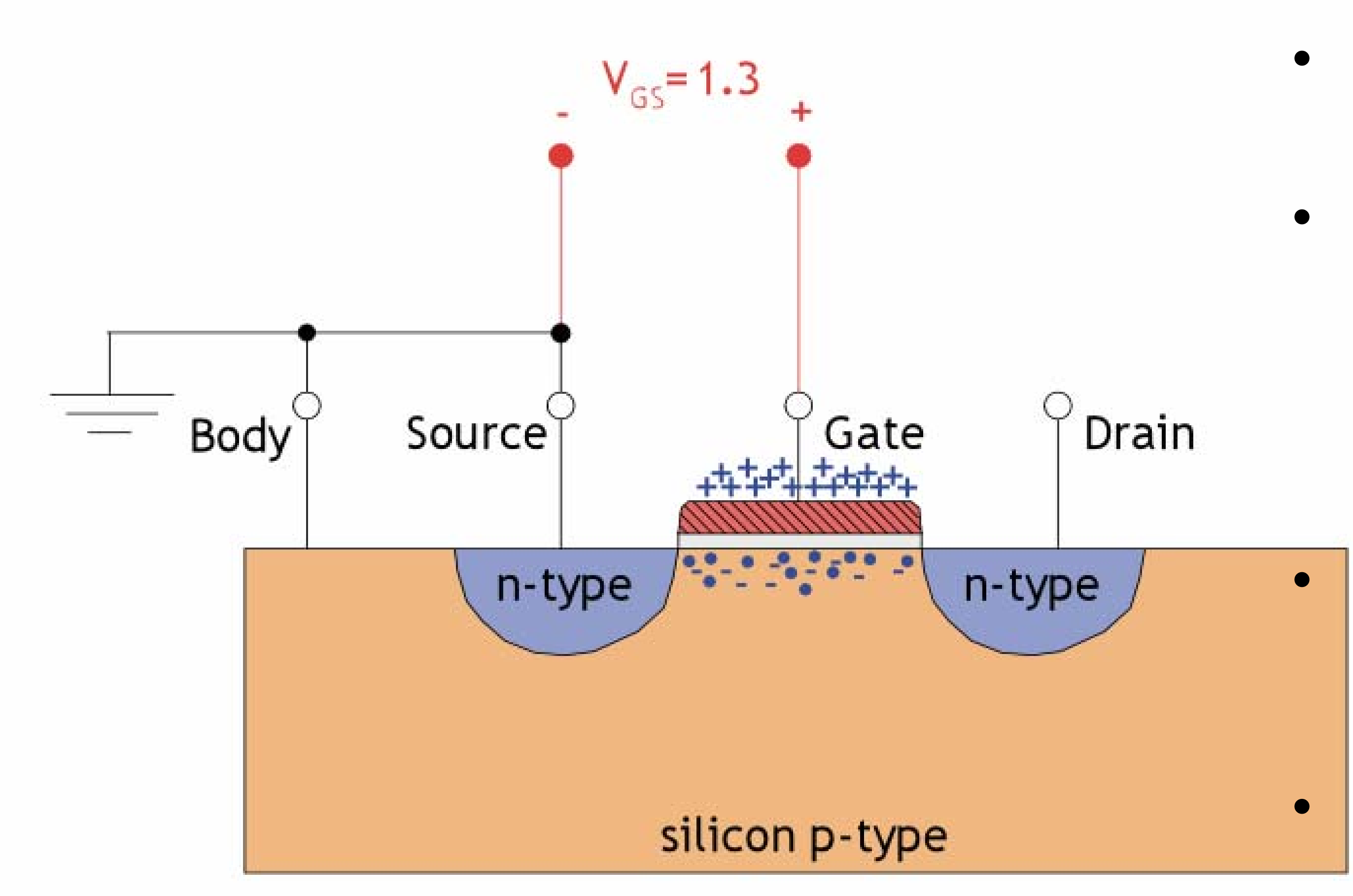
- Normally, source & body terminals kept at same potential. (V_{SB} = 0)
- When $V_{GS} < V_t$ = 1V (enhancement nMOS) there is NO conducting channel. Therefore there can be no movement of charge from drain to source; the current from drain to source, I_D = 0.

nMOS Channel Conduction



- In order to establish a conducting channel, V_{GS} (V_{GB}) must be made larger than ***threshold voltage*** V_t. When $V_{GS} > V_t$ (enhancement nMOS) an inversion layer is produced below the gate terminal.
- Channel conductivity proportional to $V_{GS} - V_t$ (***excess gate voltage***)

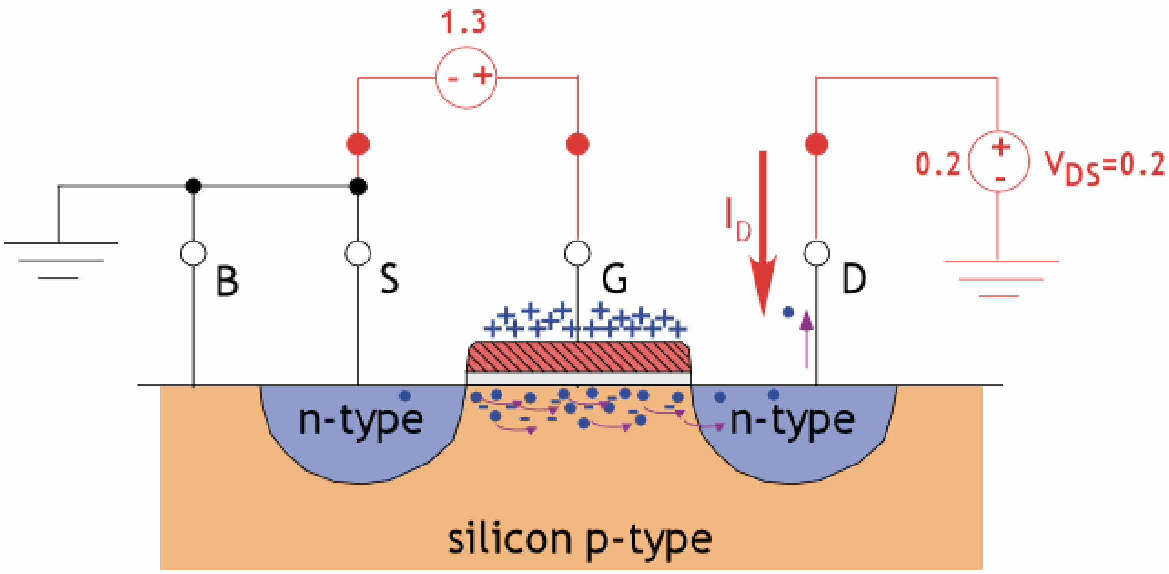
nMOS Channel Inversion Process



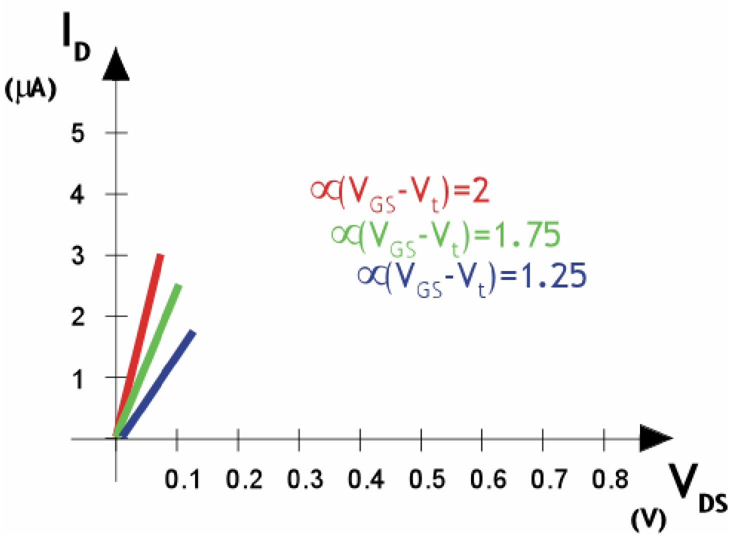
Assume V_t=1.1V

- V_{GS} = 0, no channel.
- V_{GS} = 0.5, + charges flow onto the gate, repelling holes from surface.
- V_{GS} = 1.1 free electrons attracted to surface.
- V_{GS} = 1.3, excess free-electrons connect drain and source.

nMOS – Triode



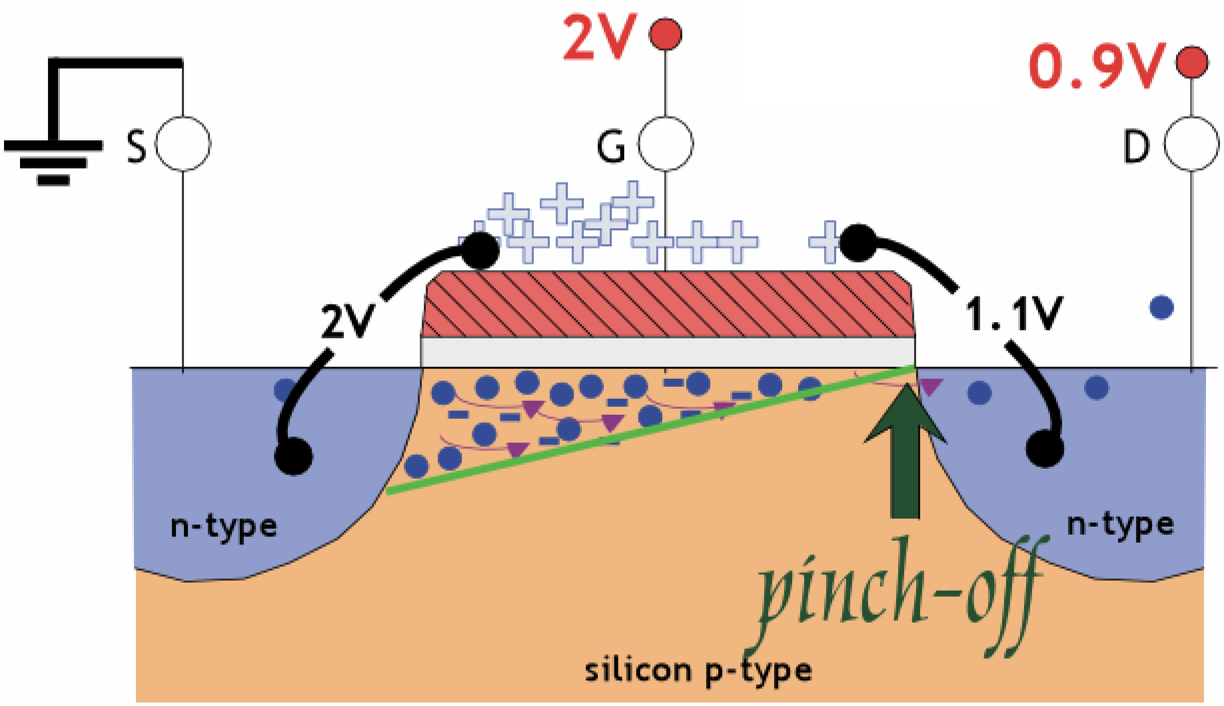
Assume $V_t=1.1V$



- Once the channel is set-up ($V_{GS} > V_t$), a small voltage between the drain and source, V_{DS}, is applied and current, I_D, begins to flow between drain and source.
- For a ***small*** V_{DS}:, current is proportional to the amount of inversion ($V_{GS}-V_t$).

nMOS Triode & Pinch-Off

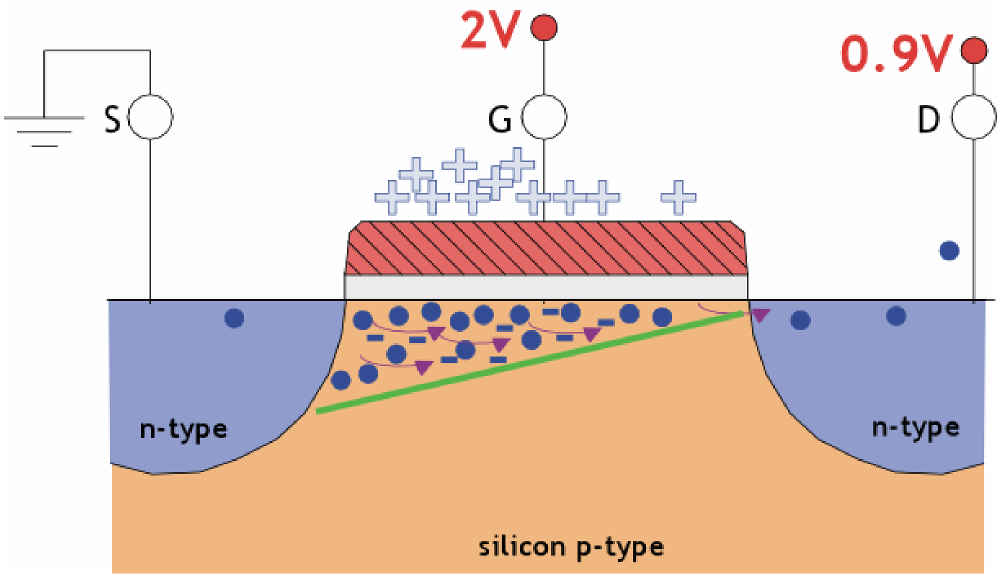
V_{DS} increased, channel shape changes



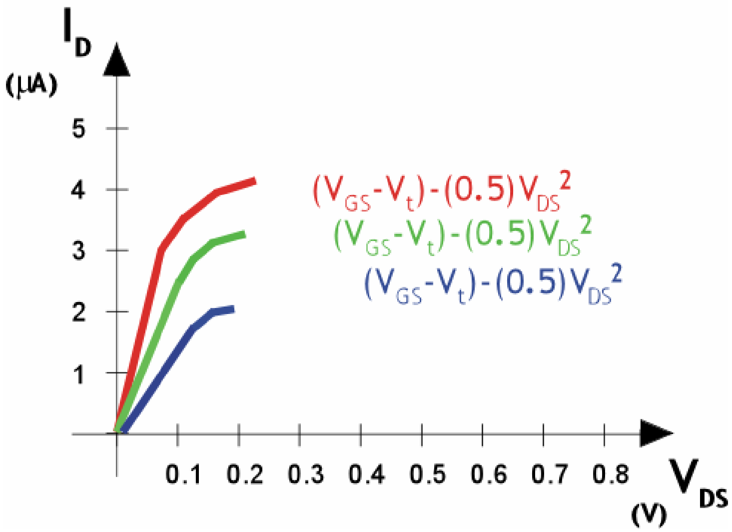
- The channel to source voltage along channel ***increases*** from V_S at S to $V_S + V_{DS}$ at D.
- The gate to channel voltage ***decreases*** from V_{GS} at S to $V_{GS} - V_{DS}$ at D.
- Channel shallower at D than S, it has a tapered shape.

I_D continues to increase up until $V_{GD}=V_t$ at a slower rate

nMOS Triode & Pinch-Off



Assume V_t=1.1V



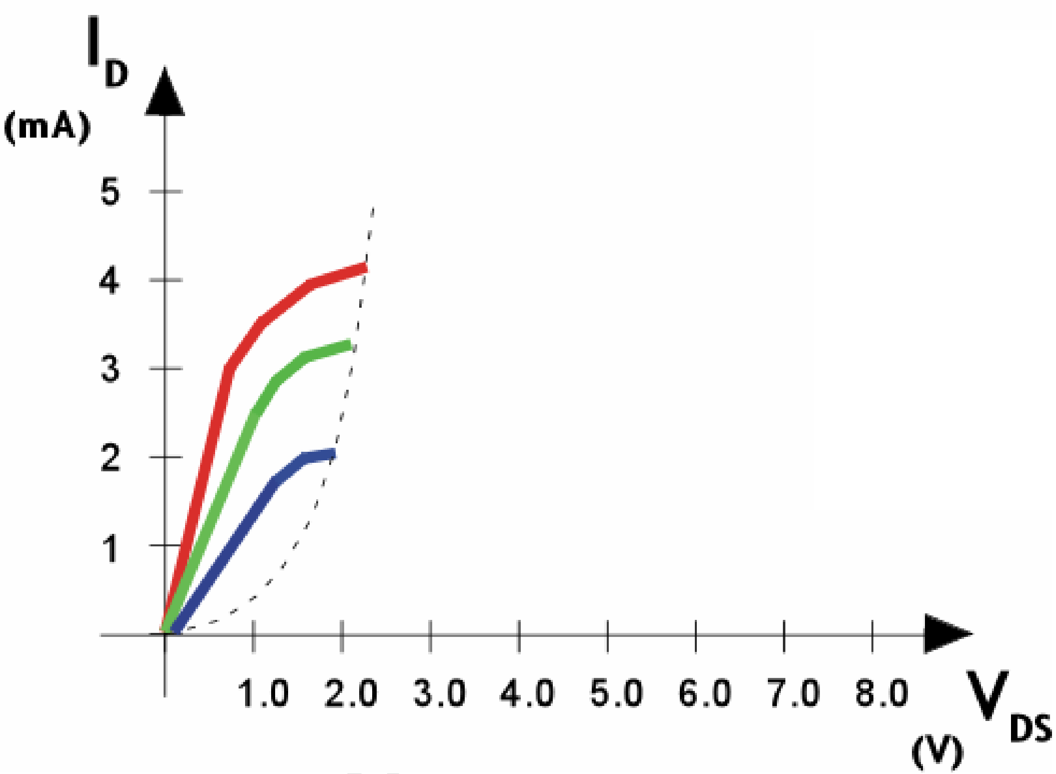
- $V_{DG} = -V_t$ at pinch-off, it is equivalently re-written as: $V_{DS}=V_{GS}-V_t$ at pinch-off.
- Triode/saturation boundary:

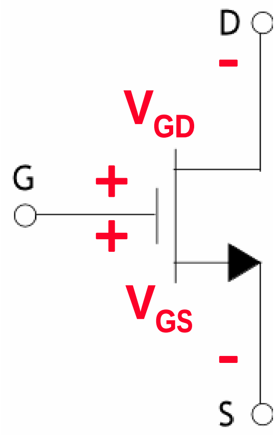
$$\boxed{V_{DS} = V_{GS} - V_t}$$

- Complete triode model includes this decreasing rate of change for I_D.

$$\boxed{I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]}$$

nMOS Triode– Summary





$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$$

$$\boxed{k_n' = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}}$$

$$\boxed{V_{DS} < V_{GS} - V_t}$$

$$\boxed{V_{GS} > V_t}$$

Triode Example:

$V_{GS}>V_t$, and $V_{GD}>V_t$

If V_t=1.1V

V_{GS}=3.2V

V_{GD}=2.2V

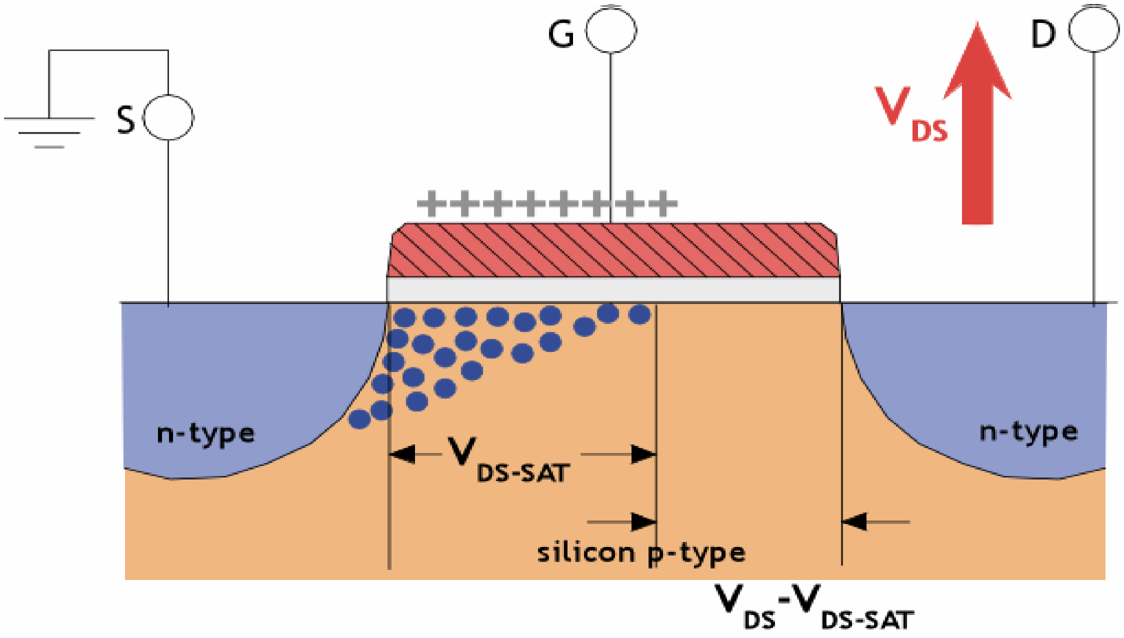
And V_{DS}=1.0V

nMOS – Saturation

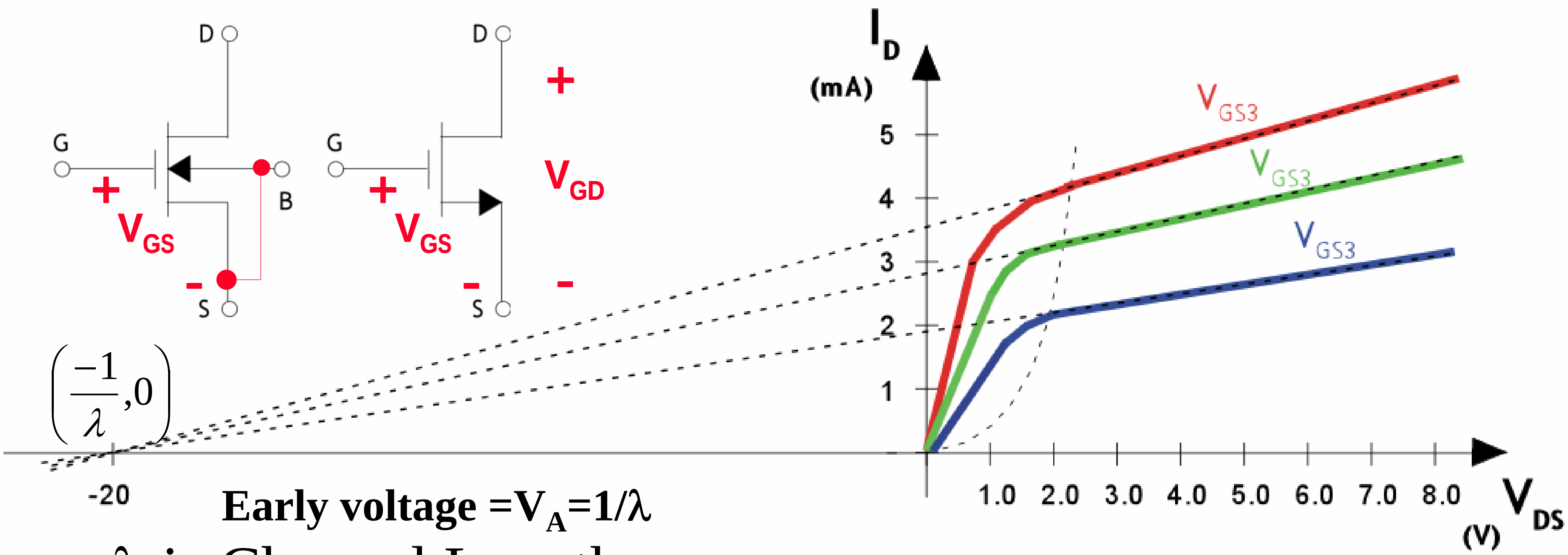
- Once channel pinch-off reached ($V_{DS} = V_{DS\text{-}SAT}$), nMOS enters saturation.
- As V_{DS} is further increased, the edge near the drain completely looses inversion and the inversion/pinch-off point starts to move towards the source.

$$\boxed{I_D = \tfrac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2}$$

- To first-order, I_D doesn't change:
  - The voltage from the source up to the pinch-off point is $V_{DS\text{-}SAT}$
  - And the excess voltage ($V_{DS} - V_{DS\text{-}SAT}$) is across the rest of the channel.



nMOS Saturation – Summary



Early voltage =V_A=1/λ

- λ is Channel Length Modulation parameter
- Typically 0.005-0.05 V^{-1}

$$I_D = \frac{1}{2}k_n^{'}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$\boxed{k_n' = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}}$$

$$\boxed{V_{DS} \geq V_{GS} - V_t}$$

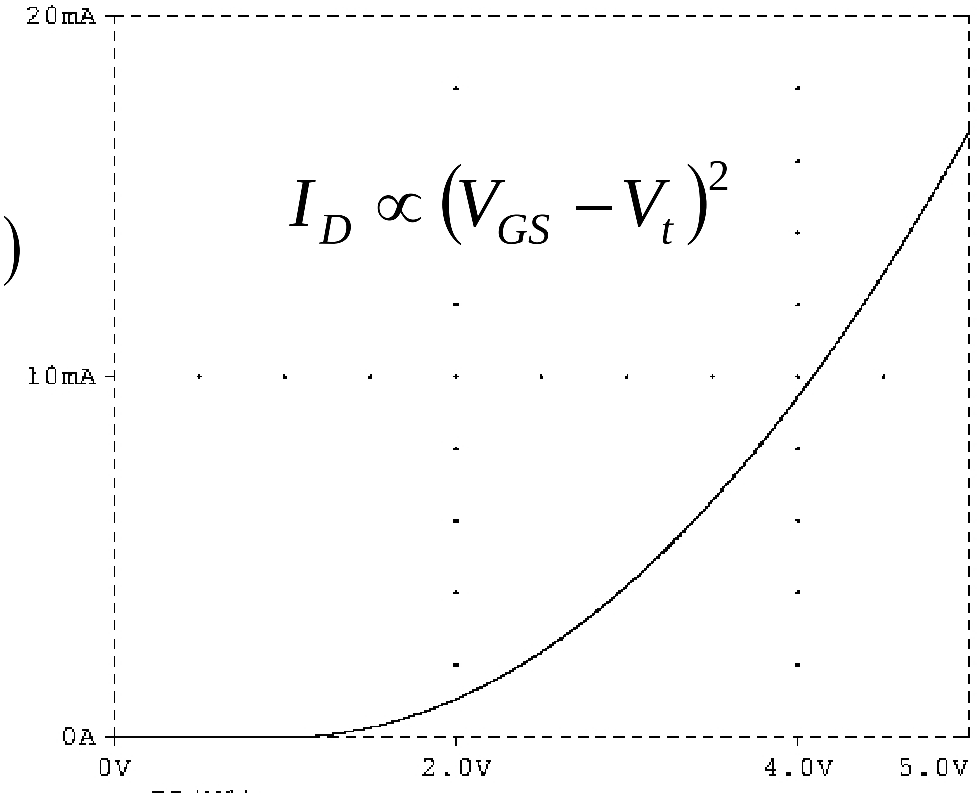
$$\boxed{V_{GS} > V_t}$$

nMOS Saturation – I_D vs V_{GS} Curve

- For constant V_{DS}, I_D vs V_{GS} is quadratic

$$I_D = \tfrac{1}{2} k_n' \frac{W}{L} \left(V_{GS} - V_t\right)^2 \left(1 + \lambda V_{DS}\right)$$

- We will see that this is analogous to I_C vs V_{BE} curve for a BJT
- MOSFET is less non-linear compared to a BJT

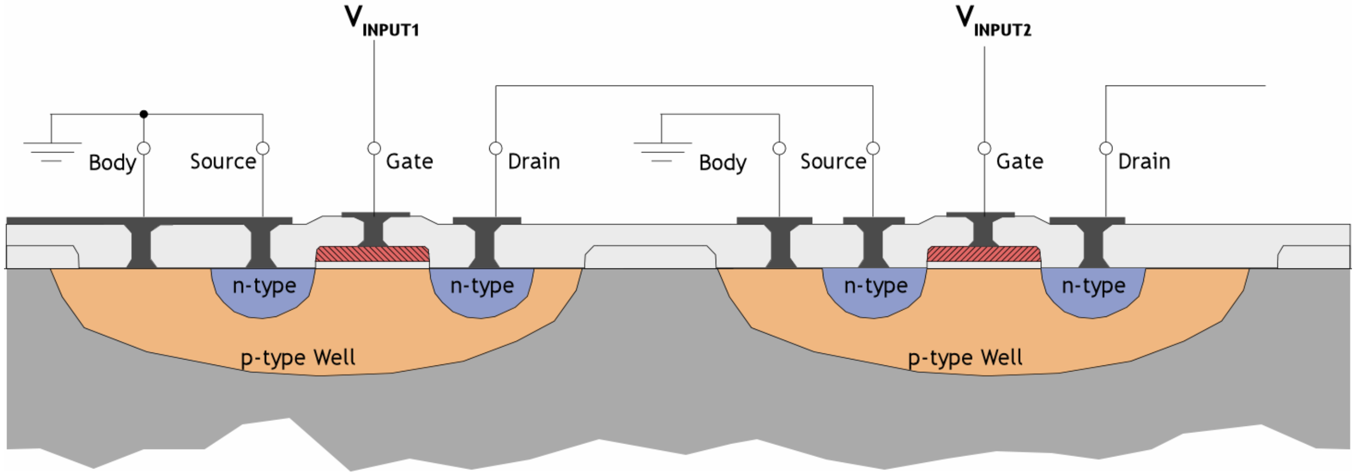


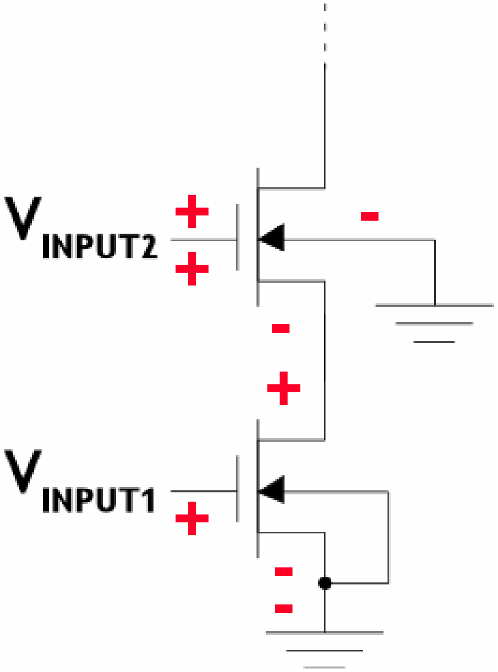
$$I_D \propto \left(V_{GS} - V_t\right)^2$$

nMOS – The Body Effect

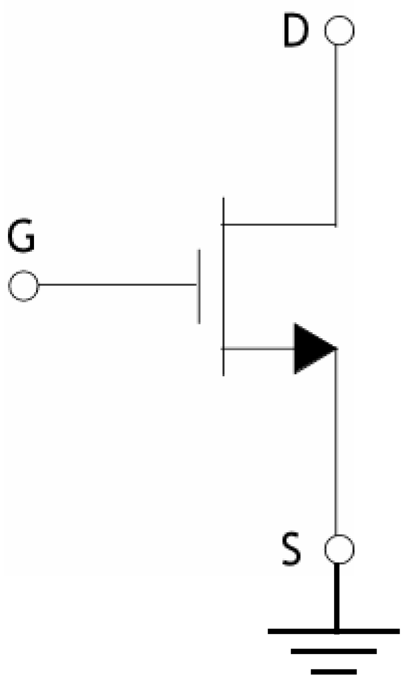
- It is not always possible to keep source and body at same potential:
  - $V_{SB} \neq 0$ accounted for in V_t
  - γ: Body effect parameter, typically $0.5V^{1/2}$
  - $2\phi_f$: Surface potential, equal to ~0.6V
  - V_{t0}: threshold when $V_{SB} = 0$

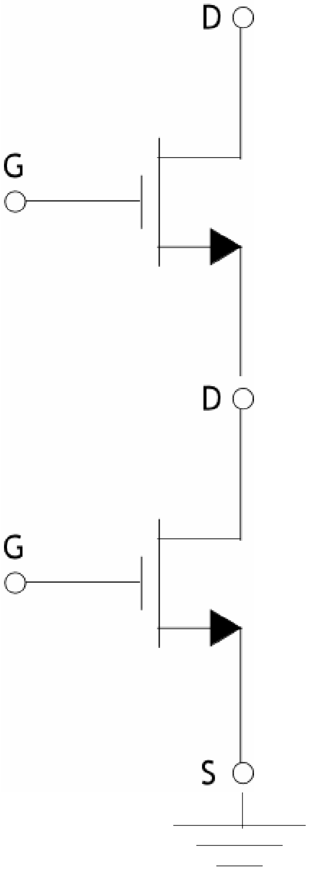
$$\boxed{V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)}$$





The Body Effect

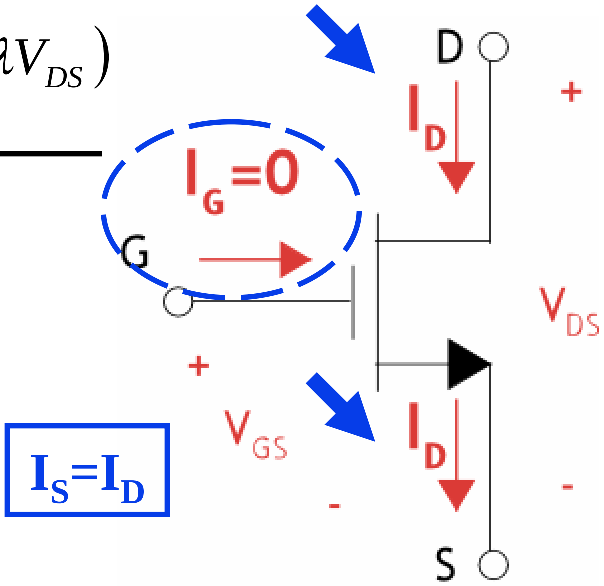




Summary of Enhancement nMOS FET I-V Characteristics

Cutoff:	$V_{GS} < V_t$	$I_D = 0$
Triode:	$V_{GS} > V_t$ $V_{DS} < V_{GS} - V_t$	$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
Saturation:	$V_{GS} > V_t$ $V_{DS} > V_{GS} - V_t$	$I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

Body effect: $V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$



$I_S=I_D$

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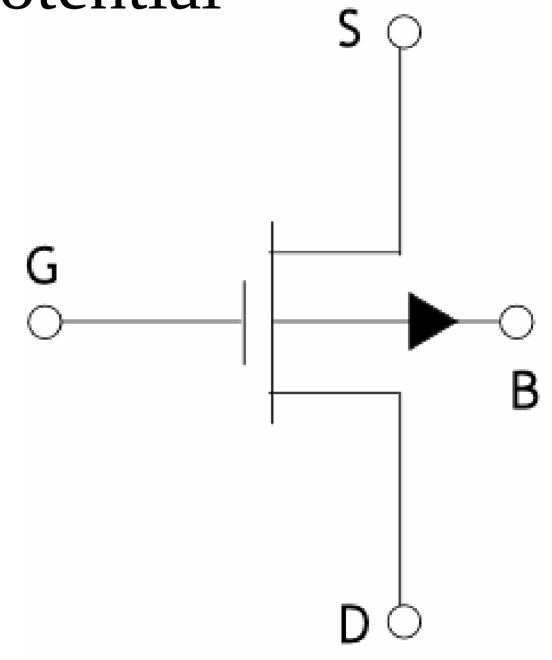
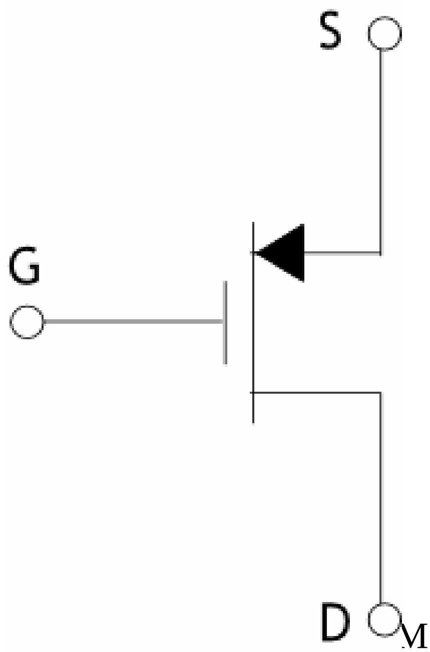
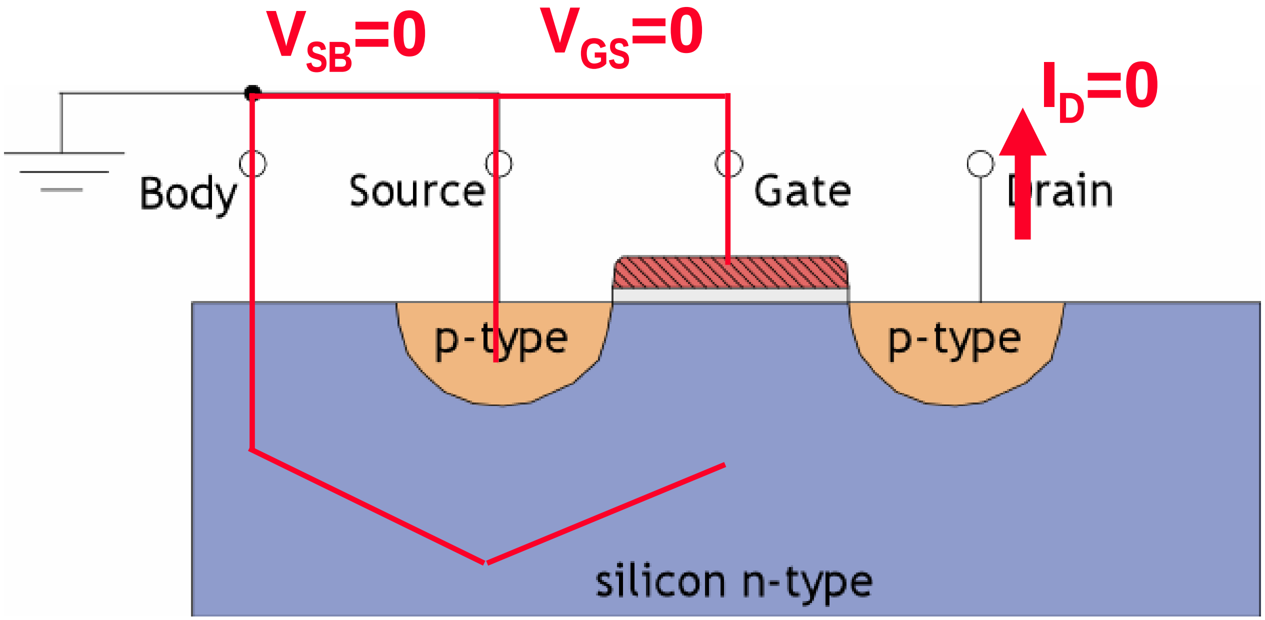


- Simplified symbol with implicit Body terminal connection
- Arrow indicates direction of current flow



pMOS Channel Cut-off



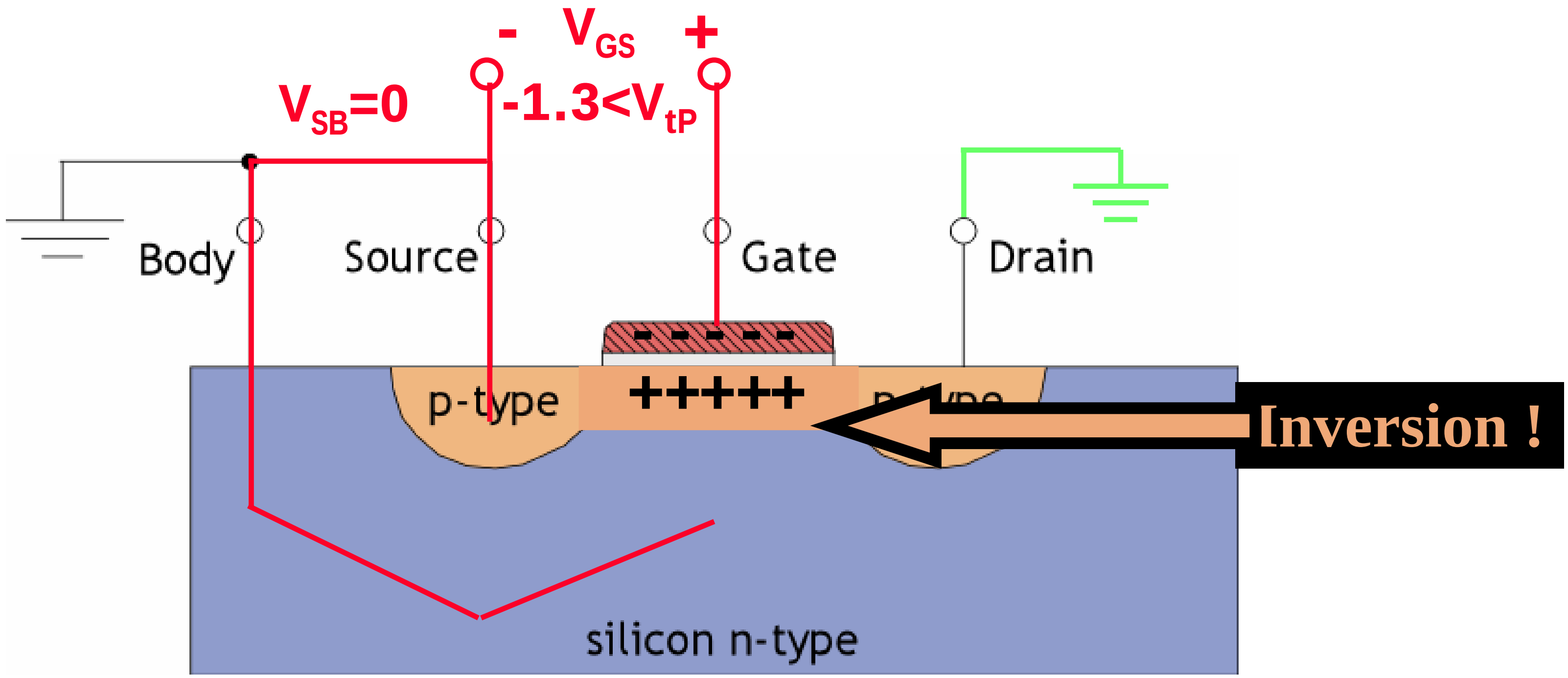
Cut-Off

$$\boxed{V_{GS} > V_{tP}}$$

$$\boxed{I_D = 0}$$

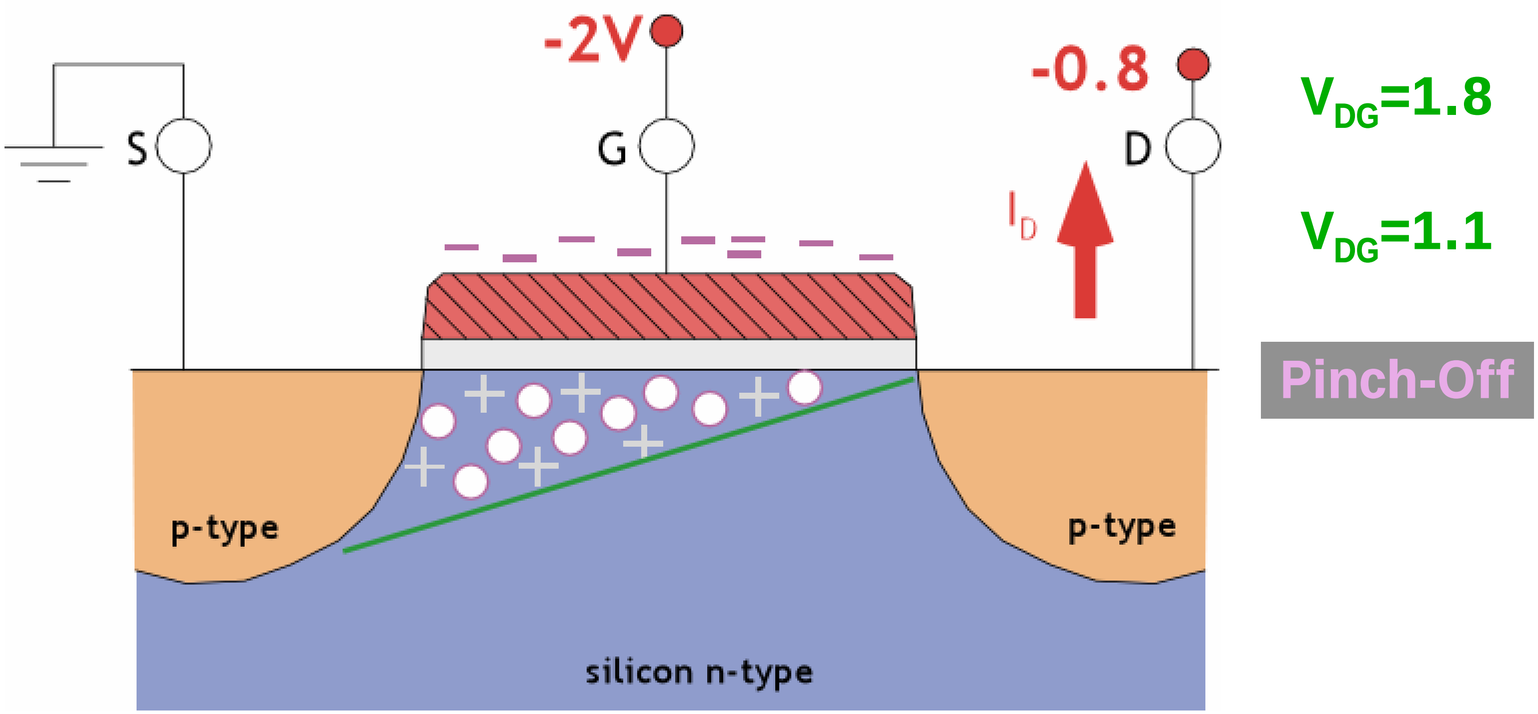
- Source & body terminals are kept at same potential. ($V_{SB} = 0$)
- When $V_{GS} > V_{tP} = -1V$ (enhancement pMOS) there is NO conducting channel. Therefore there can be no movement of charge from drain to source; the current from drain to source, $I_D = 0$.

pMOS Channel Conduction



- To establish a conducting channel, V_{GS} (V_{GB}) must be made smaller than ***threshold voltage*** V_{tP}. When $V_{GS} < V_{tP} = -1V$ (enhancement pMOS) an inversion layer is produced below the gate terminal.
- Channel conductivity proportional to $V_{GS} - V_{tP}$ (***excess gate voltage***)

pMOS Triode Region

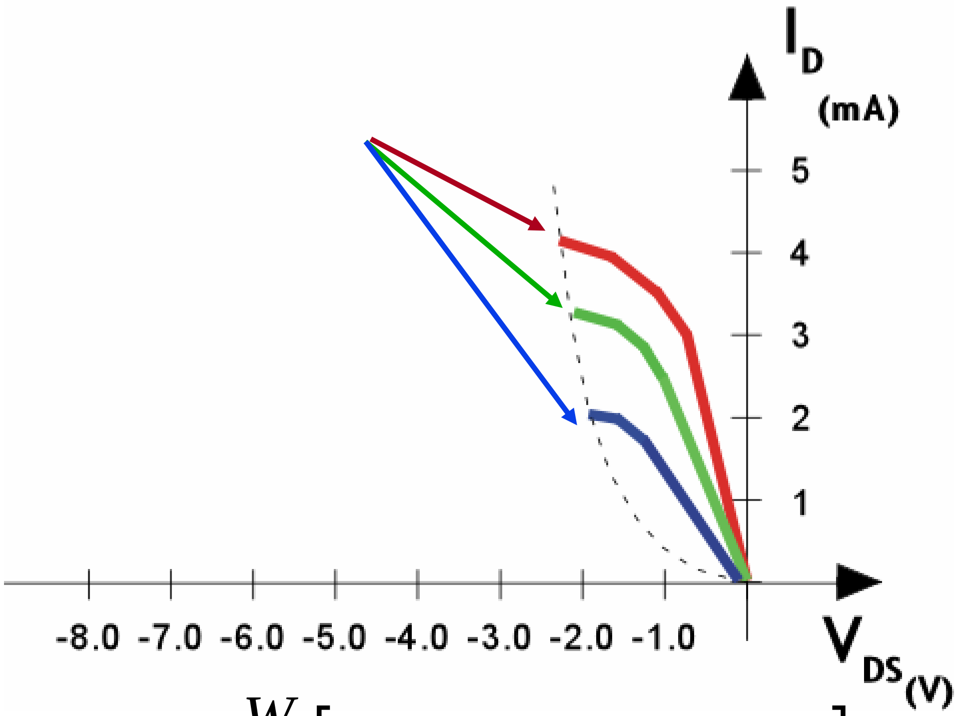


Assume V_{tP}=-1.1V

- If $V_{DG} = -V_t$, at pinch-off, then re-written: $V_{DS}=V_{GS}-V_{tp}$ at pinch-off.

$$\boxed{V_{DS} = V_{GS} - V_{tP}}$$

pMOS Triode Region – Summary

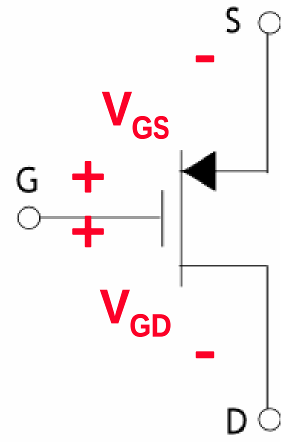


$$I_D = k'_p \frac{W}{L}\left[(V_{GS}-V_t)V_{DS}-\tfrac{1}{2}V_{DS}^2\right]$$

$$\boxed{k'_p = \mu_p \frac{\varepsilon_{ox}}{t_{ox}}}$$

$$\boxed{V_{GS} < V_t}$$

$$\boxed{V_{DS} > V_{GS} - V_t}$$



Triode Example:

$V_{GS}<V_t$, and $V_{GD}<V_t$

If V_t=-1.1V

V_{GS}=-3.2V

V_{GD}=-2.2V

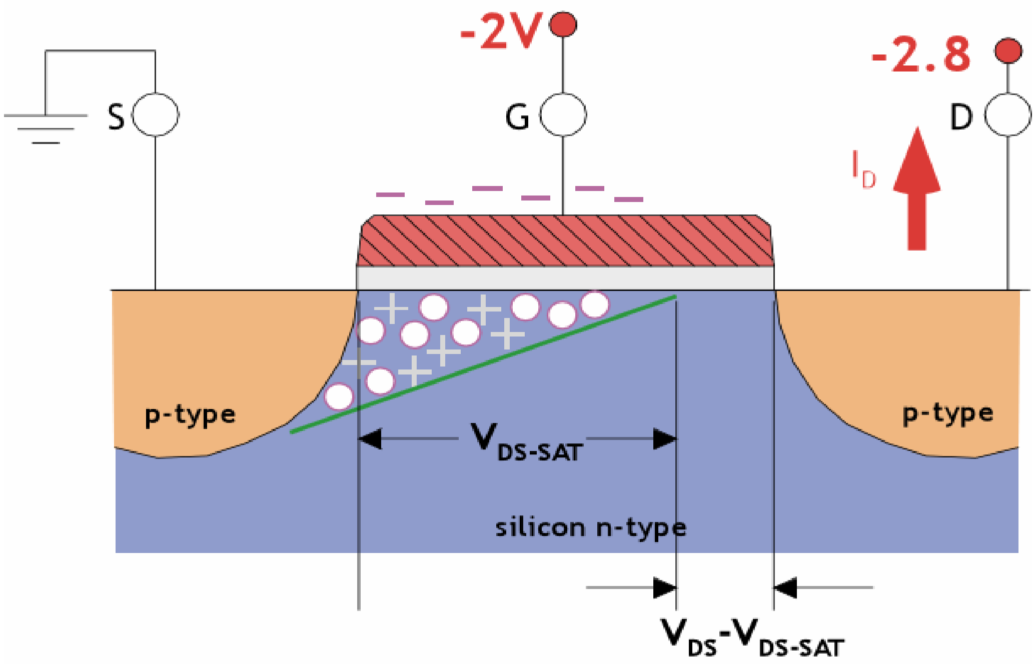
And V_{DS}=-1.0V

pMOS – Saturation

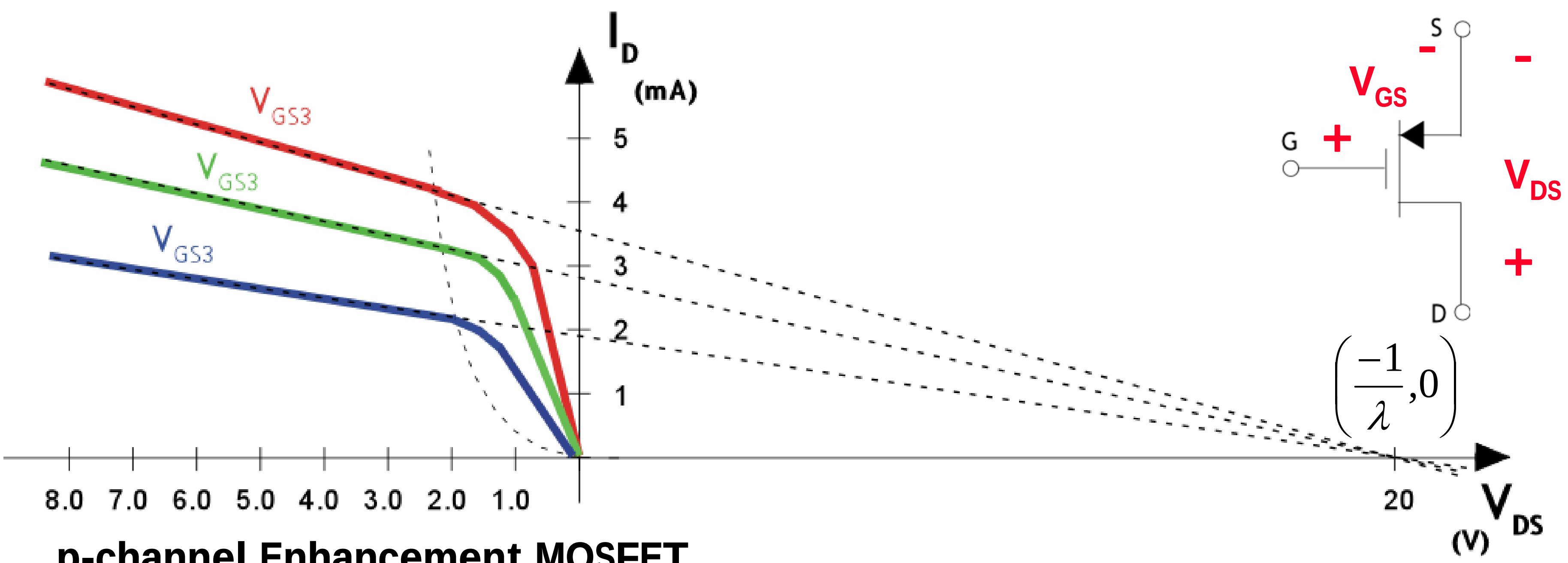
- Once channel pinch-off is reached ($V_{DS} = V_{DS\text{-}SAT}$), the pMOS enters saturation mode.
- As V_{DS} is further decreased, the edge near the drain completely looses inversion and the inversion/pinch-off point starts to move towards the source.

$$\boxed{I_D = \tfrac{1}{2} k'_p \frac{W}{L} \left(V_{GS} - V_t\right)^2}$$

- To first-order, I_D doesn't change:
  - The voltage from the source up to the pinch-off point is $V_{DS\text{-}SAT}$
  - The excess voltage ($V_{DS} - V_{DS\text{-}SAT}$) is across the rest of the channel.



pMOS Saturation – Summary



p-channel Enhancement MOSFET

- λ is CLM parameter
- λ is negative
  - typically -0.005 to -0.05 V^{-1}
  - Extrapolated curves intersect at common point.

$$I_D = \frac{1}{2}k_p' \frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

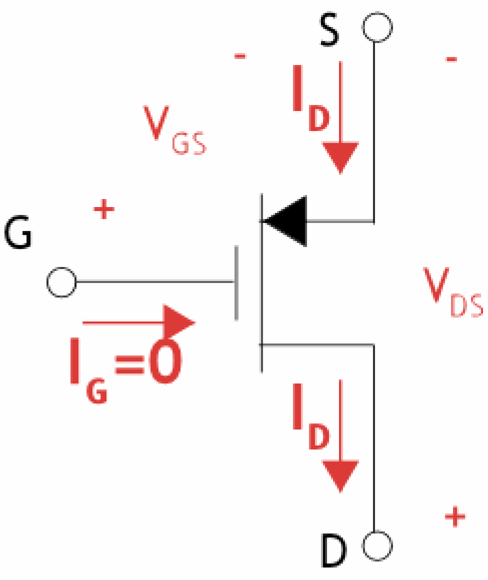
$$\boxed{k_p' = \mu_p \frac{\varepsilon_{ox}}{t_{ox}}}$$

$$\boxed{V_{GS} < V_t}$$

$$\boxed{V_{DS} \le V_{GS} - V_t}$$

Summary of pMOS FET I-V Characteristics

Cutoff:	$V_{GS} > V_t$	$I_D = 0$
Triode:	$V_{GS} < V_t$ $V_{DS} > V_{GS} - V_t$	$I_D = k'_p \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$
Saturation:	$V_{GS} < V_t$ $V_{DS} < V_{GS} - V_t$	$I_D = \tfrac{1}{2}k'_p \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$



Body effect: $|V_t| = |V_{t0}| + \gamma\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$

Note: V_{GS}, V_{DS}, V_{SB}, V_t, λ, are all NEGATIVE