Introduction to Computer Engineering I (ECSE-221)
Assignment 3: Sequential Logic
Available: Oct 20, 2006
Due Date: Nov 3, 2006

Please submit this assignment by 5pm, Nov 3, 2006, on WebCT. Your assignment must consist of two Microsoft Word documents, titled Q1-<ID>.doc and Q2-<ID>.doc, where <ID> is your student ID number; for example, "Q1-609384123.doc". The contents of each document are specified at the end of each question. In addition, your circuits, timing files, and library must be submitted via WebCT as per instructions on the site; you should create a folder just for Assignment 3, and keep all the circuit, timing files, and libraries you create for this assignment in that folder to include in your submission.

This assignment will be marked out of 100 points.

Assignments received up to 24 hours late will be penalized by 10%; assignments received up to 48 hours late will be penalized by 20%, and assignments received more than 48 hours late will not be marked.

Question 1 (50 points)

A D flip-flop is implemented using an S-R master-slave flip-flop that changes state on the falling edge of the clock. Assume that the circuit is fabricated using NAND gates with a 1 nS propagation delay.

a) Determine the set-up, Tsu, hold, Th, and propagation delay, Tpd, parameters for this flipflop. Devise an appropriate LogicWorks simulation that confirms your predictions. In the simulation, make sure to test both the case where the output changes from 1 to 0, and the case where the output changes from 0 to 1. Tsu, Th, and Tpd for the circuit are the maximums of the times you find in these two cases. See "Generating Waveforms in Logicworks" for further instructions on creating timing files.

   Your simulation should show the circuit operating correctly with the minimum possible timings, and then show the circuit failing when the timings are reduced by 1ns.

   Note: in the analysis done in class, it was assumed that the inverter connected to the clock had a propagation delay of zero. However, in LogicWorks, the inverter will have a propagation delay of 1 gate delay. This means you may get a different Tsu , Th, and Tpd for the flip-flop than indicated in the notes.

b) Compare the behaviour of this circuit to a falling edge-triggered D flop-flop. Do this using a LogicWorks timing simulation. Make sure to show how the two devices differ.

   Note that LogicWorks does not have a falling-edge triggered D flip flop. Use the device editor to change the state of the clock input by assigning the Invert.Pin attribute to the clock line. Save this new device in a library named Assign3.clf.

   When you place your new device in your circuit, set its timing parameters to match that of a D-MS FF. Select the "D" pin, and select "Simulation->Simulation Params", and set the "New Delay" to 2.99ns. This sets the Tsu of your device to 3ns. Then, select the D-FF, select "Simulation->Simulation Params," and set the device's delay to 4ns. This sets the Tpd of your device to 4ns.

c) Convert a master-slave S-R flip-flop into a J-K using the appropriate gates. Compare the behaviour of this circuit to a falling edge-triggered J-K flip-flip (the one in LogicWorks will do fine). What are the fundamental differences in switching behaviour between these flipflops? Show these in your simulation.

Note: in building your flip-flops make sure that you include a preset or clear line to fix the initial state of your flip-flops in simulation.

Submission Format:

Submit your solution to Question 1 as a Microsoft Word file entitled Q1-<ID>.doc, where <ID> is your student number (for example, "Q1-609384123.doc"). This document should include the following:

Question 1(a)

- a discussion of how you determined Tsu, Th, and Tpd for the circuit.
- an image of the circuit that you created to test your predictions.
- an annotated image of the output as shown in the Timing Window, showing the circuit working with the minimum possible timings, and it failing with the timings 1ns shorter.
- your timing file.

Question 1(b)

- an image of the circuit that you created.
- an annotated image of the output as shown in the Timing Window.
- your timing file.

Question 1(c)

- an image of the circuit that you created.
- an annotated image of the output as shown in the Timing Window.
- your timing file.

Note:

To get an image of your circuit into Word, do the following:

- In LogicWorks use Edit->Select All to select your circuit.
- Use Edit->Copy to get a copy of the circuit.
- In Word, use Edit->Paste. Your circuit will be pasted in as a graphic.

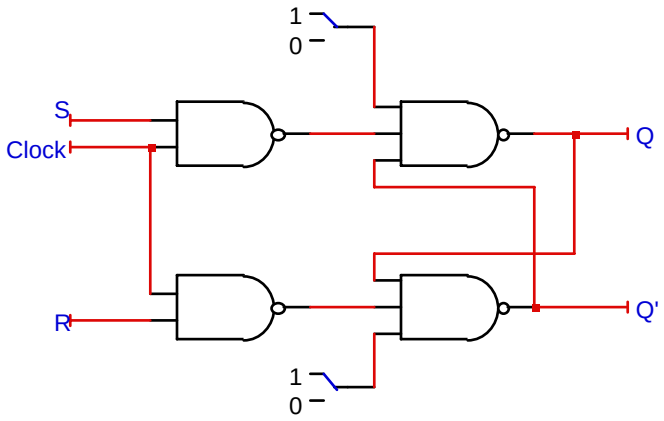
To get an annotated timing file into Word, you can do the following:

- in LogicWorks, get the Timing Window set up to show all of the timing data.
- Press Ctrl-Shift-PrtScn (or Ctrl-Shift-PrintScreen). The whole screen will be copied.
- Open a graphics program, for example Microsoft Paint.
- Use Edit->Paste.
- Get the "Selection" tool (usually a rectangle).
- Select just the contents of the Timing window. Make sure your selection includes all the signal names, as well as the timing waveforms.
- Use Edit->Copy.
- In Word, use Edit->Paste. The Timing Window will be pasted as a graphic object.
- If you like, you can annotate your timing image in the Paint program, or in Word.

Generating Waveforms in LogicWorks

LogicWorks can read in an externally generated set of timing signals for use as inputs to a simulated circuit. The format is a file of ASCII text and is described in Appendix D of the LogicWorks manual, but the following example should be sufficient to get you going for this assignment.

Consider the clocked S-R latch shown below.



In order to generate the Clock, S, and R input waveforms all you need to do is to create a text file using your favourite text editor or spreadsheet program (but remember to save the resulting file as text!). The format of the timing file is tab-delimited (i.e. separated by tab characters) text. In fact, this is particularly well-suited to spreadsheet programs like Quattro or Excel.

The timing file is in the form of a table with the first line defining the header information (remember, each entry must be separated by a tab character and each line in the file must be delimited by a carriage return). The first two entries, $T and $D, are mandatory and represent the absolute time and the delay to the next time step respectively. The remaining entries, $I Clk, $I S, and $I R, define the 3 variables for which timing information is to be generated.

$T	$D	$I Clk	$I S	$I R
0	5	0	0	0
5	5	0	0	1
10	5	1	0	1
15	5	0	0	1
20	10	0	0	0
30	5	1	0	0
35	10	0	0	0
45	5	0	1	0
50	5	1	1	0
55	5	0	1	0
60	5	0	0	0
65	5	0	0	1
70	5	1	0	1
75	5	0	0	1

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 80    5      0      0      0
 90    5      1      0      0
 95   15      0      0      0
110    5      1      0      0
115   10      0      0      0
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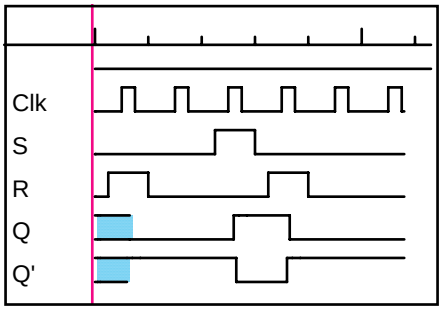
For example, the second line in the file specifies that at T=0, variables Clk, S, and R take on values of 0, 0, and 0 respectively. The D entry is 5 and specifies that the next time step will occur at T=T+5, i.e. T=5.

Once your file is prepared, use the IMPORT TIMING command under the SIMULATION menu. If the file is formatted correctly, LogicWorks will respond with the corresponding outputs once the RUN command is issued. Here is what happens when the file shown above is read in to the clocked S-R latch.



Designing the waveforms for this question requires a bit of thought! However once you get through this exercise, you should have a reasonably good understanding of the basic flip-flop types which is essential to further understanding of digital system design.

Question 2 (50 points)

It's now May, you've passed the course and managed to land a job at a company that designs and builds digital control systems. They hand you a printed circuit board that was pulled out of a 20 year old system and ask you to re-implement the circuit using current technology. There is no question of replacing the system - it has a 30 year lifetime, but the circuit board they handed you is completely fried (literally) and has to be replaced. Unfortunately there are absolutely no replacement parts or documentation available (the manufacturer is out of business). Your job - reverse engineer the circuit so that a new one may be fabricated.

The board is implemented using 7400 transistor-transistor logic (TTL). You manage to find a TTL data book and determine that the circuit is comprised of J-K flip-flops and a variety of logic gates. After poring over the board for a day you trace out the circuit diagram shown below in Figure 2.1. You are now ready to reverse engineer the circuit.

a) The first step is to determine the 6 flip-flop equations corresponding to J0, K0, J1, K1, J2, and K2 respectively. This is accomplished by tracing through the schematic. Next derive the next-state equation corresponding to each flip-flop. Use these equations to fill in the state transition table corresponding to the circuit. Also produce the corresponding state diagram.

b) The state transition table describes the logical behaviour of the circuit, but does not provide any information about timing. You look up the specifications for the circuit components and determine that the flip-flops have set-up, hold, and propagation delay times of 2nS, 2nS, and 6 nS respectively. Tpd for NAND gates is 1 nS; inverter bubbles add 0.5 nS to Tpd. Use this information to determine the maximum operating frequency of the circuit.

c) Design an implementation of the circuit using a PROM and register. Prove that your implementation is correct by devising a LogicWorks simulation that drives the circuit through all transitions in the state transition table (i.e. show the correct sequences of states for input M=0, and then again for M=1).

Submission Format:

Submit your solution to Question 2 as a Microsoft Word file entitled Q2-<ID>.doc, where <ID> is your student ID number (for example, "Q2-609384123.doc"). This document should include the following:

Question 2(a):

- the equations for J2, K2, J1, K1, J0 and K0.
- the derivation of your equations for $\hat{Q}2$, $\hat{Q}1$, and $\hat{Q}0$.
- the resulting state transition table.
- the state transition diagram (scans of hand-drawn diagrams are acceptable if legible).

Question 2(b):

- your reasoning for determining the maximum operating frequency for the circuit.

Question 2(c):

- an image of your LogicWorks circuit.
- the contents of your PROM.
- your Timing File.
- the output of your simulation from the Timing window.

Note:

To get the contents of your PROM into Word, do the following:

- In LogicWorks, select your PROM.
- Go to Simulation->PROM/RAM/PLA Wizard.
- Select "Edit Selected Device", click Next.
- Click Next again.
- Select the contents of your Prom Synthesizer window (it should be a grid of numbers).
- Press Ctrl-C to copy this data.
- In Word, use Edit->Paste. The contents of the PROM will be pasted as a table.

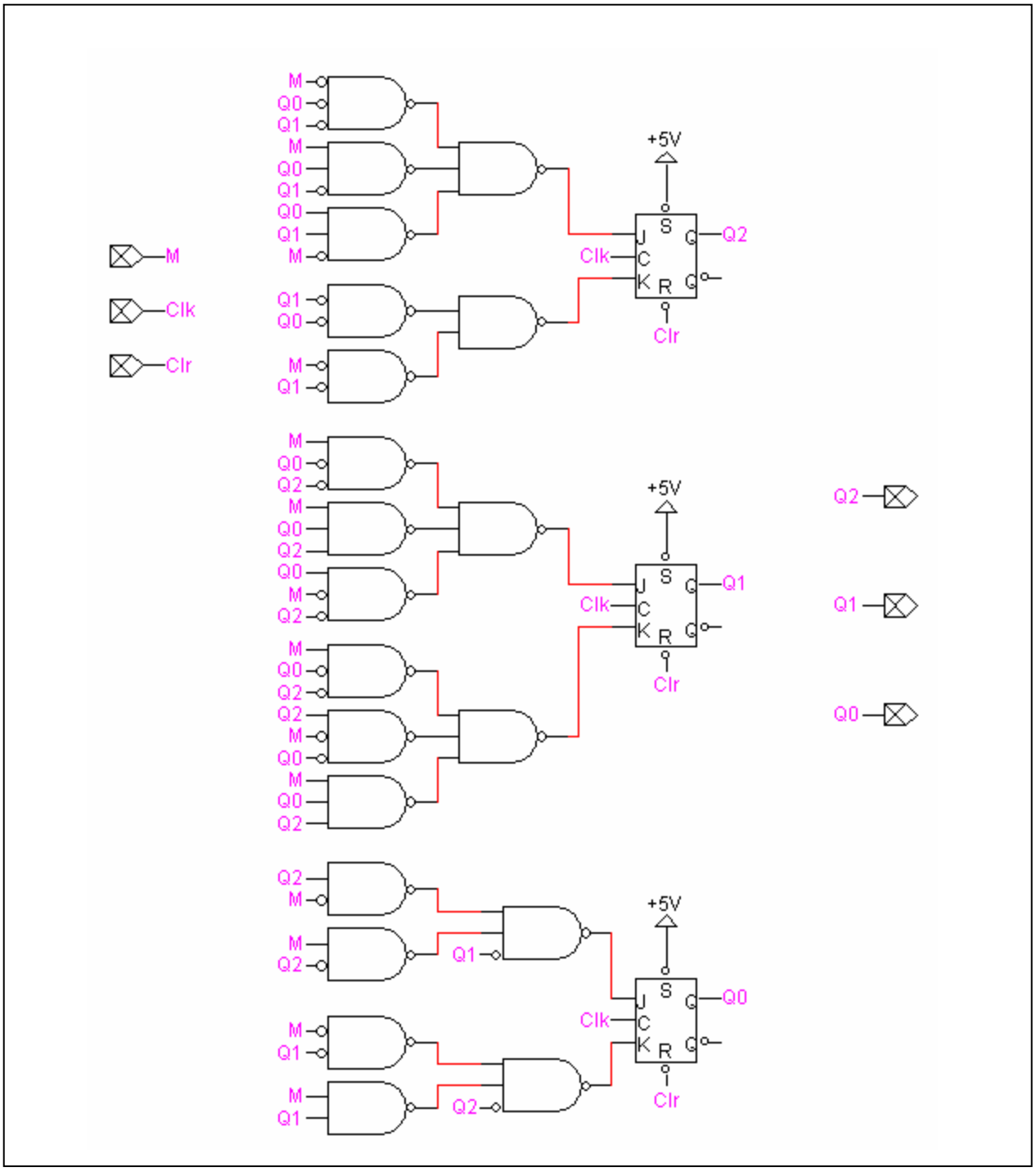

M
Clk
Clr
M
Q0
Q1
M
Q0
Q1
Q0
Q1
M
Q1
Q0
M
Q1
+5V
S
J
C
K
R
Clk
Clr
Q2
M
Q0
Q2
M
Q0
Q2
Q0
M
Q2
M
Q0
Q2
Q2
M
Q0
M
Q0
Q2
+5V
Clk
Clr
Q1
Q2
Q1
Q0
Q2
M
M
Q2
M
Q1
M
Q1
+5V
Clk
Clr
Q0
Q1
Q2

Figure 2.1