Department of Electrical and Computer Engineering

Computer Engineering

Course ECSE-322B

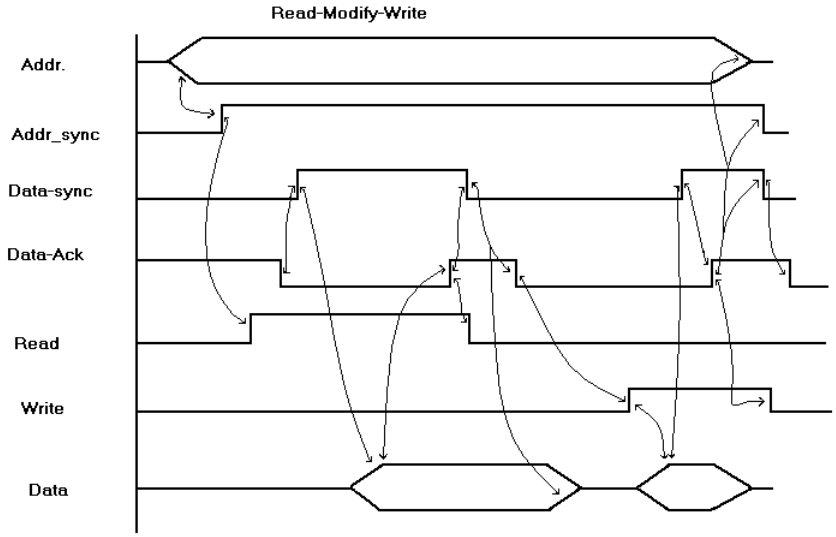
Problem Set 10 Solutions

17 March 2008

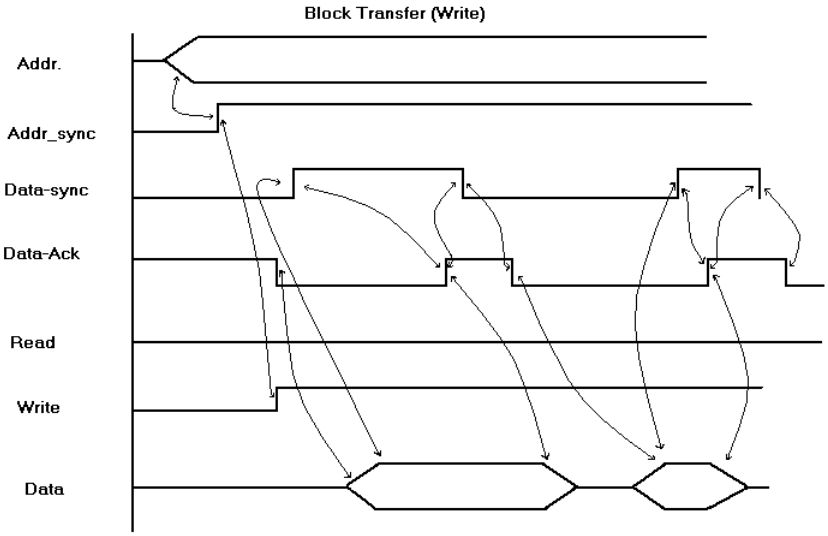
1. The timing diagram for this operation is the concatenation of two diagrams from the notes. The timing diagram for the read takes two clock cycles and then the address is changed to that of the new device and the write line is set and the data placed on the data lines. The write cycle takes one clock cycle. Thus the entire process should take 3 clock cycles.

2. The advantages of a synchronous bus are that it is simple – there is no checking between the two ends of the communication system, it is relatively robust – changes in signals and the reading of signals can only happen at a clock edge. Its disadvantages are that there is not confirmation that a transaction did not have any errors, all the devices must operate at a specified speed (i.e. within one clock cycle) or the bus will not be able to work.

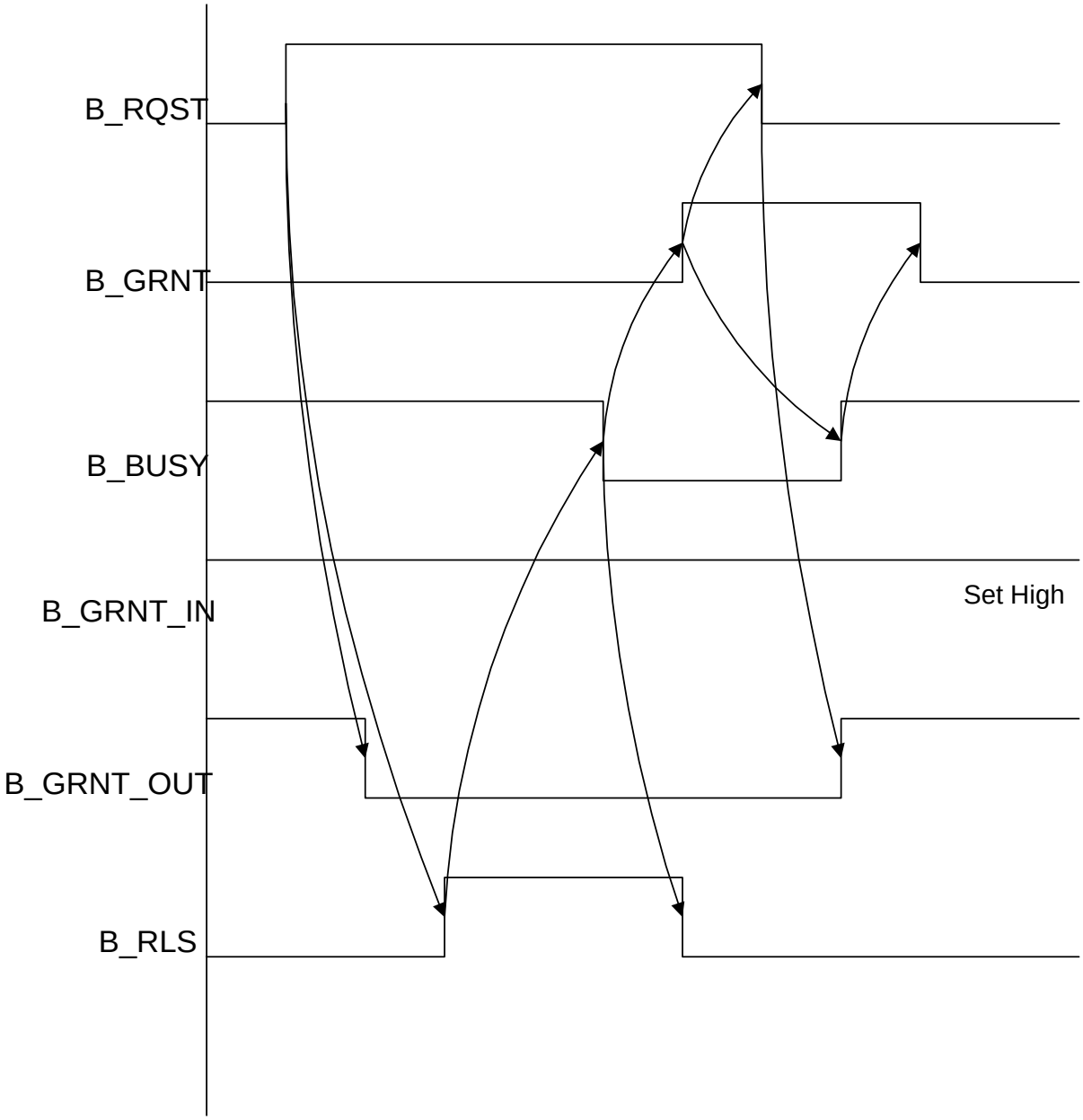
3. Draw the timing diagram for a Read-Modify-Write operation on the HGB bus



4. Draw the timing diagram for a Block Transfer operation on the HGB bus.



5. Draw the timing diagram for the operation of a single cell of the priority arbitration unit incorporating the Bus Release signal.



Note that this timing diagram assumes that the B_GRNT_IN signal is high right through this operation and that a higher priority device does not already have the bus.

6. Describe a method of implementing a fairness based arbitration algorithm

The concept of a fairness arbitration algorithm is that each device gets the bus in turn and thus, if a high priority device gets the bus and then requests it again, it cannot have access to the bus until all the other devices in the queue have had access. However, if the device has not had access to the bus at all, then it goes into the priority queue in a position dependent on its priority.

One way of implementing this system is basically with a queue structure - when a device has been serviced but requests the bus again, it goes to the end of the queue. If a device has not had the bus before (i.e. it is not currently in the queue and is not currently in control of the bus) then it is inserted in the queue in its appropriate priority structure by inserting it in the linked list.

7. Describe the difference between a non interlocked asynchronous protocol and a fully interlocked asynchronous protocol. What is the effective loss in speed of each of these protocols over a synchronous protocol?

A non interlocked protocol passes messages on the activation of signals only, thus there is no communication based on the de-activation of signals. Thus signals are de-activated based on the assumption that the operation has been successful. In a fully interlocked system, the de-activation of signals is used to signify that the operation has completed successfully.

On a rough calculation, a non-interlocked protocol is effectively 2 clock cycles longer than a synchronous system and a fully interlocked system is 4 clock cycles longer. The basis for this comparison is to assume that all the protocols are clock driven and to activate the signals at the appropriate clock cycle but to use the asynchronous message passing system.